Cadence Multi-Link PHY IP (SerDes, Analog Front-end, and DDR) to Design SoC Platform breaking the "Business Gap" on 14/16FF

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Cadence Multi-Link PHY IP (SerDes, Analog Front-end, and DDR) to Design SoC Platform breaking the “Business Gap” on 14/16FF

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This White Paper describes the new challenges going with the introduction of new FinFet based technologies and the emergence of a "business gap". Integrating Multi-links IP into a SoC allows decreasing cost of ownership, thanks to minimization of characterization and qualification efforts and optimization of IP integration, leading to shorter Time-To-Market. Flexibility offered by such IP allows thinking in term of system architecture and creating a SoC platform to address multiple applications and eventually overcome the "business gap". This paper was prepared by IPnest and sponsored by Cadence, but the opinions and analysis are those of the author.

Challenges or opportunities with 14/16nm FinFET?

Introduction of the newest technology nodes like 14nm Bulk FinFet (14FF) offers new opportunities to design System-on-Chip (SoC) addressing high performance applications like Networking or Servers to name a few, it also creates new challenges. Every time a new technology node is introduced, like 40nm after 65nm, a design team has to learn new techniques to adapt to the new node and get maximum benefit from the technology. Moving to 14/16FF from 28nm planar is not simply passing to the next node but bridging a technology gap. Double patterning has to be used on the critical process steps leading to more complex EDA treatment, the transistors are becoming very small (generating major matching challenges) and very sensitive to wide area effects.

The core and I/O supply voltages are lower, the very small transistor size induces major matching challenges, and because the transistors are very sensitive to wide area effects we discover that digital and analog calibration circuits are becoming a necessity. The economics of advanced nodes require verifying to a much higher degree of certainty than was required in earlier nodes, but the blocks are much more complicated due to the needs for calibration, running at time scales that are orders of magnitude slower

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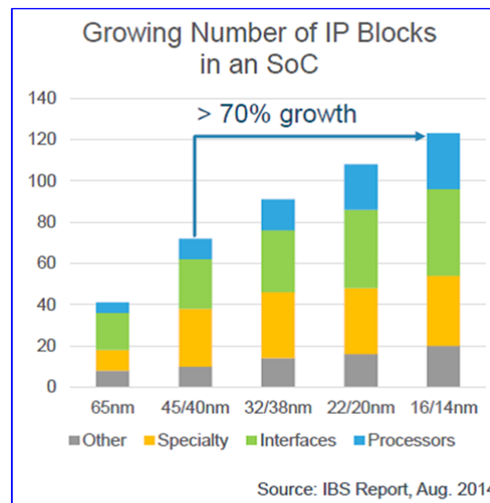
than the main path. The simulation run time is massively increased has the duration time is set by the calibration, but still using the fine scale required by the analog. The verification time dedicated to advance node designs is becoming two to three times more expansive than it used to be, due to calibration requirements. All these challenges can be overcome but lead to over-cost as more resources and more time are needed, when Time-To-Market is a critical requirement.

Emergence of a "Business Gap"

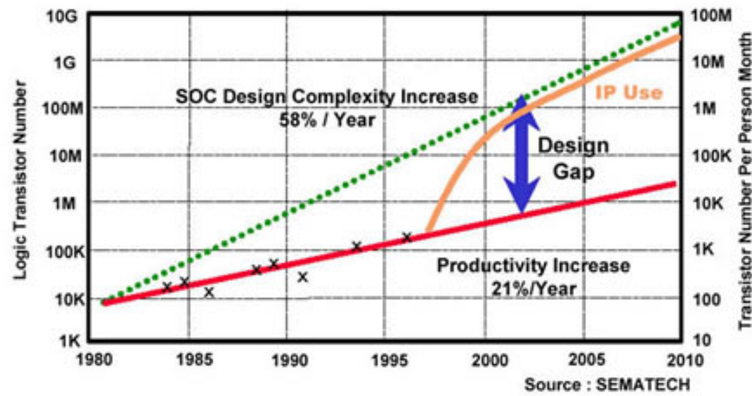
From a Silicon real estate standpoint, SoC architect will have to integrate as many functions as needed to simply fill the SoC core: most of the IC will tend to be I/O limited as the pad dimension scaling is not as effective as the transistor and interconnect scaling. This trend is leading to a major challenge, the need to integrate always more IP (see **picture 1**) in SoCs developed on emerging technology nodes.



Picture 1. IP Blocks in a SoC - this paper applies to the "Interfaces" and part of the "Specialty": AFE

Chip makers want to be the first to bring the highest possible processor performance (servers, networking), or the first to launch an Application Processor (smartphone) offering both maximum possible features, very high performances and the lowest power efficiency. Time-To-Market is a very important requirement for such devices. So the equation becomes: how to integrate 40% more IP, both analog and digital, spending two to three more time in verification, using a much more complex technology (double patterning, etc.), all of the above within the same timing envelope than on a previous node?

Designing a SoC on 14/16FF nm and below, not only means solving the above described technical issues but also finding a solution to a critical business problem linked with the increasingly high development cost. The IP reuse concept is born in the 1990's to help optimizing the chip design. Commercial IP market took off in the 2000's to solve the so-called "design gap", as designer productivity didn't grow fast enough to allow building System-on-Chip although CMOS technology scaling made it possible.



Today the semi industry is facing another gap which could be called the "business gap". Except for very few applications like mobile application processor or PC servers, the market size associated with one application is becoming too small to justify investing the huge development cost associated with a SoC designed in 14/16FF or 10FF nm. Does that mean that a majority of chip makers should give-up using advanced technologies, losing the potential benefits of higher performance and lower power and stay on 28nm or above?

Is Multi-Protocols PHY IP the solution?

Designing one unique IP able to support multiple protocols, like for example a SerDes based PHY supporting various Interface protocols like USB 3.0, PCIe 2.0 and SATA 3.0, is a proven solution. Most of the IP vendors selling mixed-signal IP are offering this capability, including Cadence with this Multi-Protocol 6G SerDes dedicated to mobile applications and supporting MIPI M-PHY 3.0, QSGMII and DisplayPort v1.2a on top of the above listed specifications.

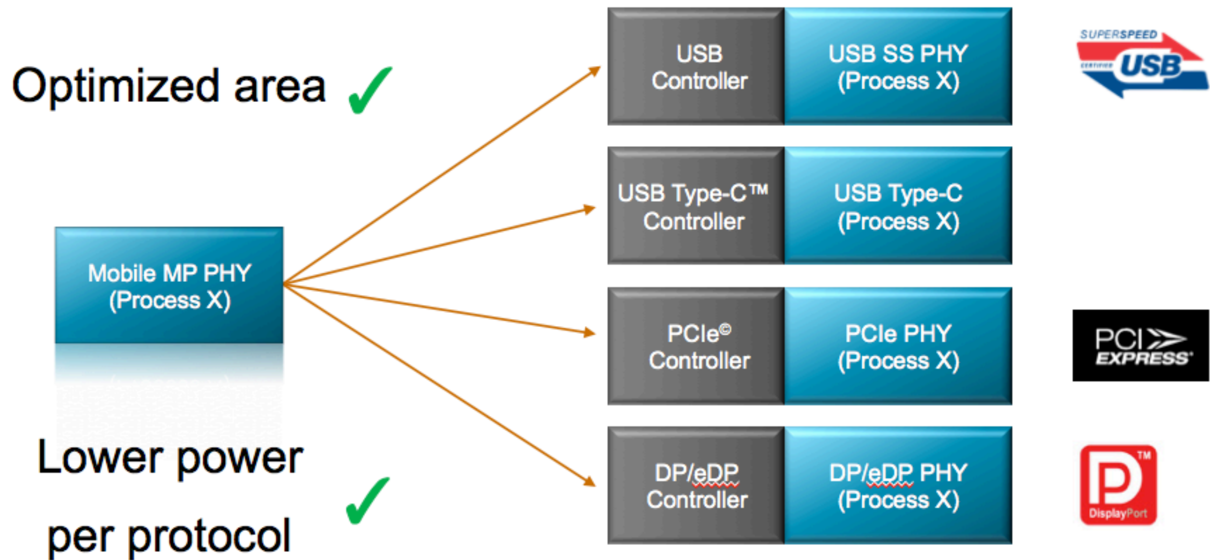


Figure 2. Multi-Protocol 6G PHY

SoC chip maker targeting mobile application will integrate the same PHY instance several time to support different protocols, and the various related controllers to personalize a specific interface link. We know that the mobile market is probably the faster moving market today. Using such a Multi-Protocol PHY is a way to build an application processor allowing rapid evolution and quickly supporting an additional protocol to comply with market demand, still using the same SoC.

Multi-links PHY IP to address the "Business gap"

If multi-protocol PHY IP has been the right answer from IP vendors to address SoC design concerns during the 2005-2015 decade, multi-link IP could be the innovative solution helping chip makers to overcome semiconductor industry challenges in 2015 and after. Flexibility offered by Multi-link IP should help to overcome the "business gap". If these huge R&D cost can be mutualized between several applications, it will become possible to address each of these market segment with a single SoC designed on the latest available technology node. Benefiting from higher performance and lower power consumption than a competitor staying on a previous node, such a SoC should be successful. We can take a real case to illustrate this new architecture leading to "One SoC for Multiple Application".

Cadence Multi-Link and Multi-Protocol

IP Design Innovation and Flexibility

- Flexibility: Multi-Protocol
  - 16G MP PHY: PCIe4/3, USB 3.1, 10G-KR, XAUI, SGMII, SATA3
- Innovation: Multi-Link
  - Single PHY to support 1 protocol or multiple
- Re-use: Multi-Application
  - One SoC to address multiple markets

Customer Example: Single SoC…

Networking: 16 Lane PCIe
Storage: 8 Lane PCIe, 8 Lane SATA
Compute: 12 Lane PCIe, 4 Lane 10G-KR
…Multiple Configs/Apps/Markets

- Value: One PHY vs. Multiple
  - One PHY vs. Multiple: To integrate, support, bring up & characterize
  - Lower risk, faster time to market, reduced integration cost, and potential area savings

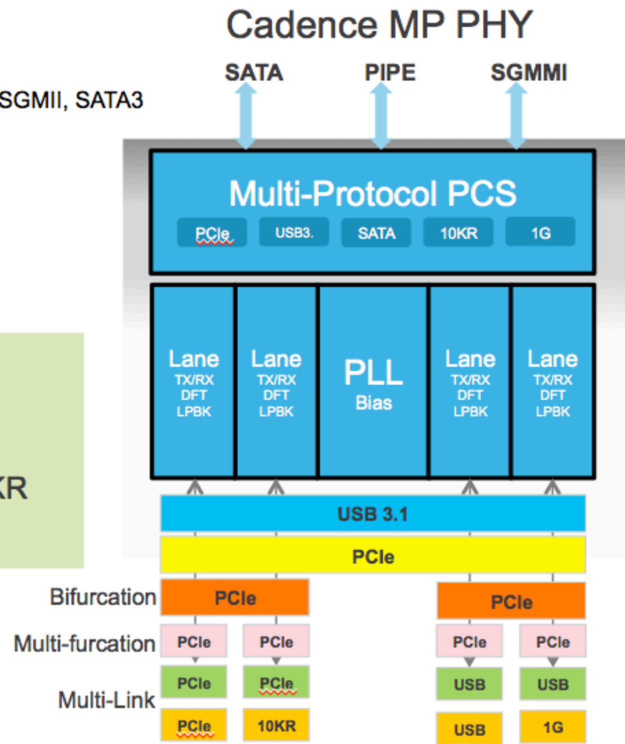


Figure 3. multiple configurations of a single SoC addressing different applications

In this example, the chip maker desire targeting networking, storage and computing application. These three market segments are related and are all demanding in term of raw performance and bandwidth capability. Targeting the most effective technology node is a must to be successful on each segment. If we mutualize the needs in term of interface protocol support, PCI Express is common to all, storage requires SATA when computing ask for 10G-KR. Re-thinking the SoC architecture in order to address networking/storage/computing and integrating Cadence Multi-link/Multi-protocol PHY IP will allow sharing the development cost and launching a unique SoC winning on each these three market, based on a SoC platform. The 16 lanes Multi-link PHY IP is configured as x16 PCIe 4.0 in the ASSP for networking, as x8 PCIe 4.0 and 8 lanes SATA 3 in the storage ASSP and the compute ASSP offers x12 PCIe 4.0 and 4 lanes 10G-KR to support 40G Ethernet. These three different ASSP are in fact based on the same SoC platform, thanks to the Multi-link PHY IP.

This is a clear advantage in term of development cost, helping bridging the "business gap". What is the impact of such Multi-link PHY IP integration on the design schedule and cost? Does it provide faster Time-To-Market?

Multi-links PHY IP, Multiple Benefits

Let's review the various activities linked with mixed-signal IP utilization. Chip maker acquiring a mixed-signal IP will run characterization to verify the electrical characteristics. To do so, a board has to be designed, integrating the IP packaged as a test chip, and measurements will be run in a lab. At design level, each IP requires integration effort. Once the prototypes are released, extensive chip qualification has to be done, measuring HTOL, verifying latch-up sensibility and ESD strength, on every functional I/O. Finally, when a Physical Design Kit (PDK) has to be updated, each physical IP core needs to be updated.

Activity	Single protocol Serdes	Multi-protocol Serdes
Porting	6 x {porting, TO, testing}	1 x {porting, TO, testing}
Characterization	6 x {board, package, setup}	1 x {board, package, setup}
Integration	6 x effort of single serdes integration	1 x effort of single serdes integration
Qualification	6 x {HTOL, latch-up, ESD}	1 x {HTOL, latch-up, ESD}
PDK update	6 cores that need to get updated	Single core that need to get updated

Figure 4. Multi-Link Physical IP Activity List

Even if IP integration allows to strongly improving productivity, it's becoming one of the most resource intensive task during SoC design. Understanding and integrating one IP supporting one protocol represent time and resources investment. Integrating a Multi-link physical IP (SerDes or Analog Front End) to support N different links allows reducing this integration effort by a factor equal to N: when this Multi-link IP is instantiated N times, the effort stays the same. This benefit directly impact the design resource utilization, it also shorten the integration phase and the Time-To-Market (TTM).

IP characterization, done in parallel with chip design, is resource consuming (board design, lab setup,…) and impact the project cost. Characterizing one IP only allows mutualizing cost and resources when characterizing the multiples supported protocols, and minimized the global cost. The same principle applies to qualification, resource and hardware consuming. Using Multi-protocol/Multi-link IP allows minimizing the overall project cost, due to test equipment or resources.

IP vendor is getting an important benefit too. Designing and maintaining a single IP instance instead of several will allow this IP reaching maturity and acquiring robustness faster. Such a benefit is also highly profitable for the chip maker sourcing this IP, as it decrease the potential risk of failure linked with IP usage.

These benefits positively impact the chip maker risk and cost of ownership linked with such multi-link PHY IP. What is the effect on the SoC ecosystem, along the supply chain? At the foundry stage, qualifying this PHY requires releasing only one Multi Project Wafer (MPW) die only, instead of several MPW, leading to

cost reduction (only one tape out is required) and faster enablement. Moreover the TTM advantage is also valid for the foundry as it can get earlier revenues from devices in production.

This concept of Multi-link IP is not restricted to SerDes and is perfectly valid for Analog front End (AFE) IP designed to support various wireless radio protocols. Let's take as an example an ASSP designed to support wireless radio for IoT application. IoT is an emerging field of application and nobody can be 100% sure about which radio protocol will be effectively dominant. Developing one wireless radio platform based on a Multi-link AFE IP could be a safe solution, allowing saving a new tape out when the industry will move to a different protocol.

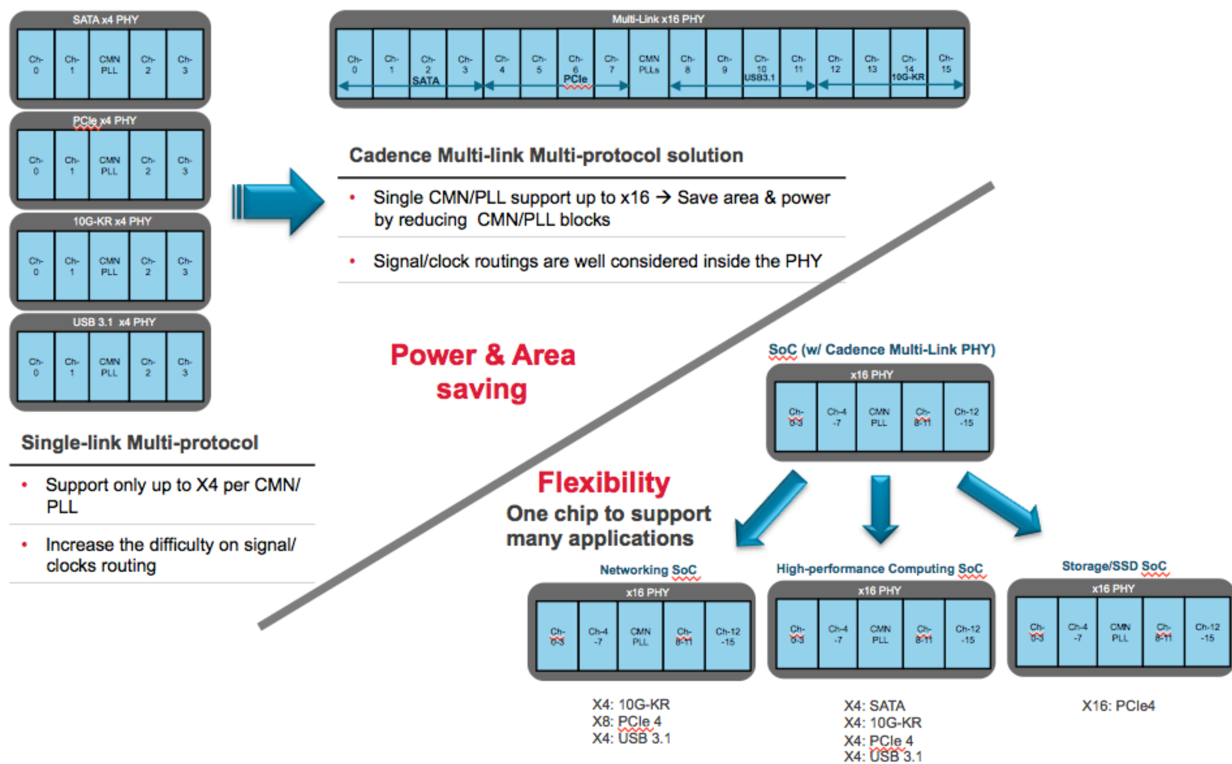


Figure 5. Power & Area saving with Multi-Link PHY

Technology nodes like 14/16FF are offering incredibly high gate density in the core, when the number of I/Os tend to grow to support always more interface protocols based on wider bus. The net result is an I/O limited IC. You can add logic gates at almost no cost, integrating various controllers to support multiple protocols, but the PHY design has to be optimized. Cadence Multi-link solution allows such optimization as we can see on the above example. Instantiating several single-link (Multi-protocol) PHY require one common block including PLL (CMN/PLL) by X4 link, when such CMN/PLL can support up to X16 lanes in a

multi-link. Reducing the number of CMN/PLL to one instead of four allows saving 10% area, reducing the I/O ring perimeter and directly impacting the chip area.

Multi-link IP create system architecture opportunity

We have reviewed the various benefits, immediate, visible and measurable cost or resource savings that bring Multi-protocols/Multi-links IP integration into one SoC. Even if it's difficult to put measurable value on it, flexibility is another strong advantage that such IP brings. To derive value from flexibility, chip maker will have to be creative and rethink architecture, moving from chip level architecture to system level architecture. As of today, one Application Specific Standard Part (ASSP), or one SoC, was designed to target one application only.

Multi-Protocol 16G Serdes

Market Segment	Protocol	Data rate (Gbps/lane)	Infrastructure MP Serdes
Infrastructure	PCIe©4	16	✓
	PCIe3	8	✓
	PCIe2	5	✓
	USB 3.1	10	✓
	USB 3.0	5	✓
	10G-KR	10.3125	✓
	RXAUI/XAUI	6.25 / 2.5	✓
	QSGMII/SGMII	5 / 1.25	✓
	CEI-11/CEI-6	11 / 6	✓
	SATA3	6	✓

Figure 6. 16G Multi-Protocol PHY Standard Support

To exploit flexibility, chip makers can build SoC platform, targeting several applications with a single SoC. Obviously, these applications should be related enough, like in the above described example of a platform SoC designed to target storage, networking and computing. Multi-link physical IP is a new concept, and it will require changing the way you architect a system in order to target multiple applications with the same SoC. Being creative, a chip maker building a SoC platform addressing multiple application will break the

"business gap" and be able to play and win when more conservative competitors will stay stuck on previous nodes.

Conclusion

Moore's law evolution is generating a "business gap", designing a SoC on advanced technology nodes requires such high investment that the return may not be guaranteed if you target only one application. A conservative approach would be to keep designing on affordable nodes, 28nm or above, but it would prevent to benefit from extra performance and lower power, known to be the keys of success. Moving from chip architecture, one SoC targeting one application, to system architecture and creating a SoC platform allowing targeting several applications with the same SoC may break this "business gap". This new approach is made possible by the flexibility offered by Multi-link PHY IP (SerDes or AFE).

For such IP, the Cost of Ownership is cheaper, as the various cost and resource intensive activities like IP integration, characterization setup and board design, qualification or PDK update are done only one time, leading to faster SoC design. Shorter TTM can be a priceless advantage for SoC addressing highly competitive markets. Such a Multi-protocols/Multi-links PHY IP offering CoO and TTM benefits all along the supply chain from fabless to foundries and EDA ecosystem.