

Design IP for USB Type-C Port Controller

Overview

Introduction of USB Type-C™ connector, USB 3.1 and USB Power Delivery 2.0 specifications is driving new applications in emerging mobile and consumer products. Cadence® way is going forward with an IP core that implements the Cadence Design IP for USB Type-C Port Controller compliant with relevant USB specifications. The Controller IP enables management of a Type-C subsystem that may include USB 3.1 IP for data transfer rates of 10Gbps, Power Delivery IC for up to 100W power output and DisplayPort™ 1.3/1.4 support for up to 8K video output resolution.

The Controller IP targets USB Type-C connector applications that make full use of USB Power Delivery 2.0 and USB Type-C Alternate Modes. The Controller IP provides the necessary functionality to enable Type-C connector support, Power Management IC control, and support for both USB and DisplayPort protocols.

The I2C interface of the Controller IP provides support for an external MCU, while an ARM® AMBA® APB interface interfaces to embedded controller or main applications processor.

The Controller IP is delivered with an API to ease integration into the target application. The Controller IP is silicon proven and has been extensively validated with multiple hardware platforms.

The Controller IP is part of the comprehensive Cadence Design IP portfolio comprised of interface, memory, analog, and systems and peripherals IP.

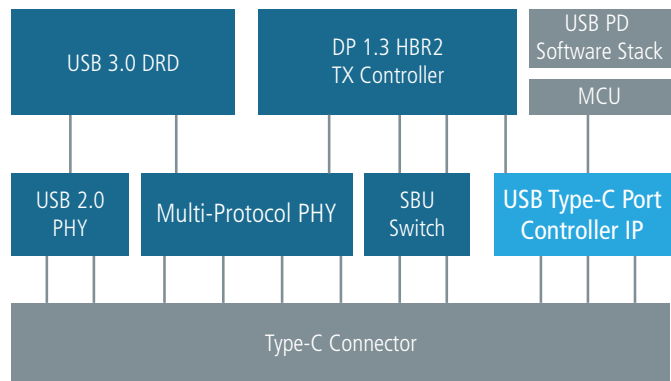


Figure 1: Example System-Level Block Diagram

Benefits

- **Specification compliance speeds up system development and time to market**
- **Support for Alt Modes and Power Delivery enables new applications**
- **External and embedded controller support provides system flexibility**

Key Features

- Power Delivery support for up to 100W of power through external Power Management IC
- Up to 10Gbps of data transfer when integrated with USB 3.1 IP
- Support for 8K video through DisplayPort 1.3/1.4 Alt-Mode
- Standard I2C or ARM AMBA APB interfaces for external or embedded controller interfaces
- Compliant with USB Type-C Cable and Connector, Power Delivery and DisplayPort Alt-Mode specs
- Good CRC generation

Product Details

The Controller IP implements lower layers of PD communication in a Type-C application. Optionally, the TCPC Controller can work autonomously by advertising itself based on value of strap pins.

The Controller IP is using a small processor-equipped system, the firmware (FW) of which is preloaded into its instruction RAM.

Additional hardware modules accelerate some tasks so the real-time requirements put on firmware are low. These implement the following functions:

- CRC calculation
- BMC encoder
- BMC decoder

The APB slave interface provides access to an emulated register set. This is a custom register set defined within The Controller IP specification. It is emulated by the embedded processor within its data memory space.

The embedded processor utilizes Special Function Registers (SFR) mapped into its data memory to control and monitor the TCPC-defined interfaces, including its interfaces to the PHY part of the Controller (TCPD PHY). This includes an APB Master Interface to enable control of TCPD-PHY.

The wakeup detection logic within The Controller IP detects activity on the APB slave interface and the Type-C PHY interfaces, which enables the FW to effectively stall waiting on events relating to Type-C configuration.

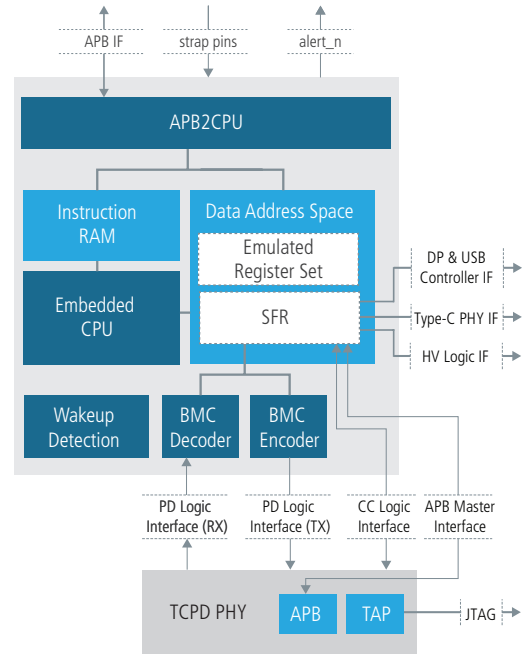


Figure 2: IP-Level Block Diagram

Various defined events relating to Type-C configuration are signaled to the system by asserting the interrupt interface.

Availability

The Controller IP is available with various configurations and supports the following protocols:

Protocol	Speed	Process node
USB 3.0, DP 1.3 HBR2	6G	TSMC 28HPC
USB 3.1, DP 1.3 HBR3	10G	TSMC 16FFC

Related Products

- Cadence Dual Role Device Controller IP for USB 3.0
- Cadence IP for DisplayPort TX Controller
- Cadence 6Gbps Multi-Protocol SerDes PHY IP
- Cadence 10Gbps Multi-Protocol SerDes PHY IP

Deliverables

- Synthesizable RTL
- Testbench
- Synthesis and simulation support files
- GDS for PHY
- Documentation

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