

Transitioning to USB Type-C with DisplayPort: Key Design Considerations

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Our electronic devices are on the verge of becoming even simpler to use and maintain, with the emergence of USB Type-C™ Cable and Connector Specification. With the adoption of USB Type-C along with the USB Type-C Alternate Modes (Alt Modes) and USB Power Delivery specifications, we will likely see more electronic devices that operate on a single cable for charging, data transfer, and video output. What are the key design considerations when transitioning from the legacy cable standards to this current one? In this paper, we will provide a primer on what you need to know to design for, and take advantage of, the market opportunities presented by USB Type-C and DisplayPort (which is enabled by USB Type-C Alt Modes).

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Introduction

Apple's newest MacBook has a single USB Type-C port for charging, data transfer, and video output. Google's Chromebook Pixel is also one of the first devices to debut a USB Type-C charger. Before long, we will likely see more electronic products on the market with similarly streamlined cabling schemes.

Each year, roughly three billion USB ports are shipped.¹ The USB Type-C Cable and Connector Specification is bringing new excitement to the venerable standard, erasing the limitations of legacy USB Type-A and Type-B plugs on today's smaller and mobile devices. USB Type-A connectors, with their flat, rectangular shape, are typically found in host devices like desktop computers, laptops, and gaming consoles. USB Type-B connectors, available in several shapes, stick out of peripherals like printers and external hard drives.

USB Type-C connectors, on the other hand:

- Support reversible plugs with two-way insertion; the host and device connectors are the same
- Enable higher data rates, up to 10Gbps for USB Type-C 3.1 Gen2
- Facilitate increased power, up to 100W through support for the USB Power Delivery 2.0 specification
- Offer bi-directionality, so that devices can provide and consume power
- Support scalable power charging, which means that power consumption may dynamically change depending on the application's needs
- Can eventually replace all other connectors by using USB Alt Modes

Designing for USB Type-C devices requires meeting emerging specifications, new power delivery targets, and verification requirements. This paper discusses what you need to know to integrate USB Type-C, USB Power Delivery 2.0, and USB Alt Modes (primarily the DisplayPort standard) into your designs, and offers suggestions to mitigate the design challenges.

Enabling a Single Functionally Rich Cable

Starting this year, USB Type-C replaces all USB connectors. Compliance with USB Power Delivery 2.0, supporting power delivery of up to 100W, makes USB Type-C connectors suitable for charging electronic devices. And through USB Alt Modes, currently supported by the DisplayPort 1.2 and MHL specifications, USB Type-C connectors will be able to connect to displays.

In the past, USB has won the market over FireWire (IEEE 1394) by providing only slightly less performance at a much lower Bill of Material (BOM) price. Cost considerations are still very important—the Type-C connector is only slightly more expensive than legacy connectors. Unless very high performance is needed—such as via an interface like PCI Express®—USB Type-C will fit well into many design plans, particularly for cost-sensitive mobile devices such as phones, tablets, portable drives, and low to mid-level notebook computers. For those seeking ultimate performance, Thunderbolt 3 will be the connection of choice. Now, switching from miniDP to a Type-C connector, the latest revision of the graphics and movie artists' beloved standard delivers data transfer speeds up to 40Gbps together with support for PCIe Gen3, USB 3.1 Gen 2, and DisplayPort 1.2. So, Thunderbolt 3 provides a much higher performance package that will come at a much higher cost and, because of this, will likely remain a minority choice. USB also specified Audio Accessory and Debug Accessory Modes for the Type-C cable. As you can guess, these modes enable digital audio pass-through, eliminating the need for a 3.5mm audio jack in the future, as well as accessing the device firmware and debugging it via a special mode.

USB Type-C Design Requirements

Compared to its predecessors, USB Type-C (see Figure 1 for a functional model) comes with some unique design requirements:

- Pull-up, pull-down resistors at configuration channel (CC) pins
- Capability to provide supply at VCONN
- Connection and marked cable detection, cold-socket, and VCONN control circuitry
- Switches to provide VCONN/Rp to CC pins (downstream-facing port (DFP))
- Control to turn off/on supply to VBUS
- Switch to connect SS_TX/SS_RX to TX1/RX1 or TX2/RX2

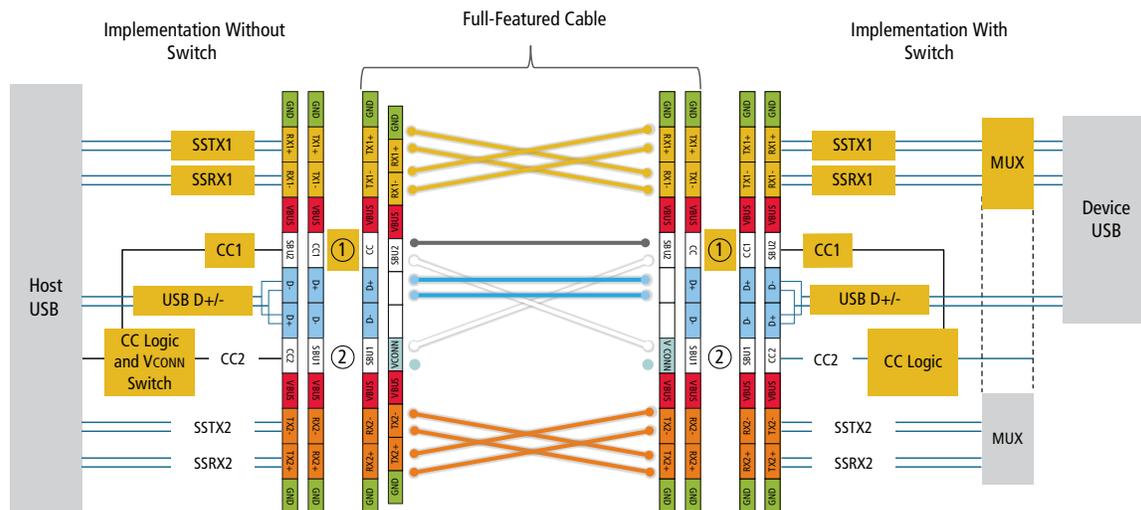


Figure 1. USB Type-C functional model

Challenges for System Integrators and Chip Developers

These requirements translate into some new design challenges for system integrators. Additional pins, for example, are needed to support the specification's flip connector. This, in turn, impacts the design's architecture and, hence, the BOM. As a universal connector, a USB Type-C design would need to support multiple protocols. Its architecture would also need to support power delivery mechanisms.

For chip developers, there are some PHY considerations to take into account. Flexibility is key, in order to support multiple protocols, including those to come. To comply with multiple protocols, the PHY would need to support a wide electrical specification range, particularly on the equalization side (CTLE or DFE, for example). Given this, a single analog PHY can be ideal in terms of area and performance.

Chip developers may opt to go with smaller processes for a digital advantage; however, advanced nodes can severely limit the type of supply voltages that you can use, as well as the type of devices that are available to meet electrical requirements of Type-C and power delivery. Consider processes at 28nm and below. Here, sub-1V core devices and 1.8V I/O devices are the norm. As a result, supporting 3V and above in the existing die becomes a big bottleneck, unless multi Vt and expensive additional mask sets are used. Minimizing costs and supporting such platforms requires many circuit techniques to circumvent the reliability issues related to electrical overstress.

Verification becomes more complex when designing for USB Type-C. New components in the mix mean new dependencies. There's also a new level of integration hierarchy to consider, with alignment and integration of system interfaces. And, of course, more supported protocols mean more protocols to verify. Systems which need to verify the main link with the CC-PHY and power delivery I/O will need complex mixed-signal environments to verify the complete system. The modeling of analog components (described either in Wreal or Verilog-A) with other digital Verilog stubs pose a challenge to verification engineers.

Higher Data Rates Call for Architectural Adjustments

Let's spend a moment discussing the higher data rates that USB Type-C supports, as this will also impact your architecture. USB 3.1 Gen 2 delivers data rates up to 10Gbps, and USB Type-C supports USB 3.1. End devices that support different speeds will use the same lanes, so you'll need to make sure that your architecture is designed such that the bus will be saturated—particularly when both USB 3.1 Gen 1 and Gen 2 are transferring data.

While USB 3.1 Gen 1 features 8-bit by 10-bit encoding, USB 3.1 Gen 2 has an encoding scheme of 128 bits by 132 bits, resulting in much less overhead, better bandwidth, and some enhancements to the data packets. Since both USB 3.1 Gen 1 and Gen 2 use the same lanes, the USB Implementers Forum (USB-IF) has developed a more effective means of discovering the maximum speed at which the link between two devices can operate. The low-frequency periodic signal (LFPS) has been modified into the LFPS-based Pulse Width Modulation Messaging (LBPM), which ensures that the devices can talk to each other and negotiate speed even before the link is trained.

With the USB 3.1 Gen 2 link layer comes a second traffic class for asynchronous data packets. This second traffic class allows isochronous transmission to be prioritized so that it has a better chance of meeting the bandwidth requirement. Future releases of the USB specification will also operate on the same lanes. To ensure that bandwidth isn't diminished when an application is receiving data from faster as well as slower devices, the USB-IF has established multiple INs—the ability to ask multiple devices for data, one after another, without having to wait to receive it. When supported by both devices and hosts, multiple INs increases performance by eliminating Not Ready responses and facilitates saturation of the bandwidth.

Design Considerations for DisplayPort Specification

Given the prominence of video in today's electronic devices, the ability for USB Type-C connectors to connect to displays is an important development. This capability is made possible by USB Alt Modes, which is supported by the Video Electronics Standards Association's (VESA's) DisplayPort digital display interface. The combination of DisplayPort and USB Type-C brings full DisplayPort audio/video performance at up to 8K at 60Hz. In addition to connecting video sources with display devices, the standard also can be used for other forms of data, including audio.

Designing USB Type-C applications with support for the DisplayPort standard comes with two key challenges: interoperability and compliance. The design itself is not terribly complex, particularly on the controller side. However, to future-proof your design, you'll need to ensure that the design can maintain interoperability throughout the lifecycle of the end product.

Bringing USB Type-C Together with DisplayPort Standard

There's strong market potential for designs that meet not only the USB Type-C specification but also support the 100W power delivery capability via the USB Power Delivery 2.0 specification and the DisplayPort standard via USB Alt Modes. Plus, if the newest MacBook and the Chromebook Pixel are any indication, the market is indeed ready for the versatility of a functionally rich next-generation cable. To address the design challenges involved with meeting each of these specifications, consider an IP subsystem approach.

By using pre-verified IP blocks integrated into a subsystem, you can avoid the time and effort involved in verifying otherwise separate components and in ensuring that each component will work well together. To future-proof your design, seek PHY IP that can support not only USB and DisplayPort but other existing as well as emerging protocols. Firmware on the controller that can be modified can meet evolving or changing protocol specifications. The IP should ideally handle a wide range of power and be able to communicate with external power management IC up to 100W and internal power management IC up to 15W of 3A over 5V, as defined by the Medium and High Current Modes of the USB Type-C Cable and Connector Specification.

Cadence's USB Type-C/DisplayPort IP Subsystem

Cadence offers an IP subsystem (Figure 2) with pre-verified components, including a port controller IP that integrates USB Type-C, USB Alt Modes, and USB Power Delivery. The subsystem, which enables development of single-chip solutions that combine video, audio, USB, and up to 100W of power delivery on a single external connector, includes:

- A connector-agnostic USB controller
- A DisplayPort 1.3 transmitter controller
- A 6G multi-protocol SerDes PHY
- And a USB Type-C port controller with an embedded Tensilica® Xtensa® CPU

The IP subsystem is designed to deliver competitive power, performance, and area (PPA), along with fast time to market. It is:

- Standards compliant, meeting the USB Type-C, USB 3.1 Gen 1, USB On-the-Go (OTG), and USB Power Delivery specifications, as well as the DisplayPort 1.2a specification at 5.4Gbps per lane
- Easy to integrate into your design, providing a single IP top for accelerated time to market, reference drivers for USB, DisplayPort, and TCPC specifications, flexible firmware-based TCPC implementation, and interoperability with major USB power delivery stacks

With this subsystem, users can configure the individual pieces, such as the number of ports, slots, and specific ARM® AMBA® AXI configurability features for the host functions. The subsystem also features some configurability options:

- Individual IP configurability
- Unified AMBA APB and AXI configuration interfaces
- USB only, USB/DisplayPort, and DisplayPort four-lane operation

In particular, the AMBA AXI configuration interface enables you to mitigate risks of system latency that can affect performance of the USB controller. The support in the AXI interface for outstanding transactions allows the system to divide the data entering the USB controller into smaller chunks that can be buffered inside the controller. The data is then transferred when there is time available for the USB controller on the main system bus, making better use of system bandwidth.

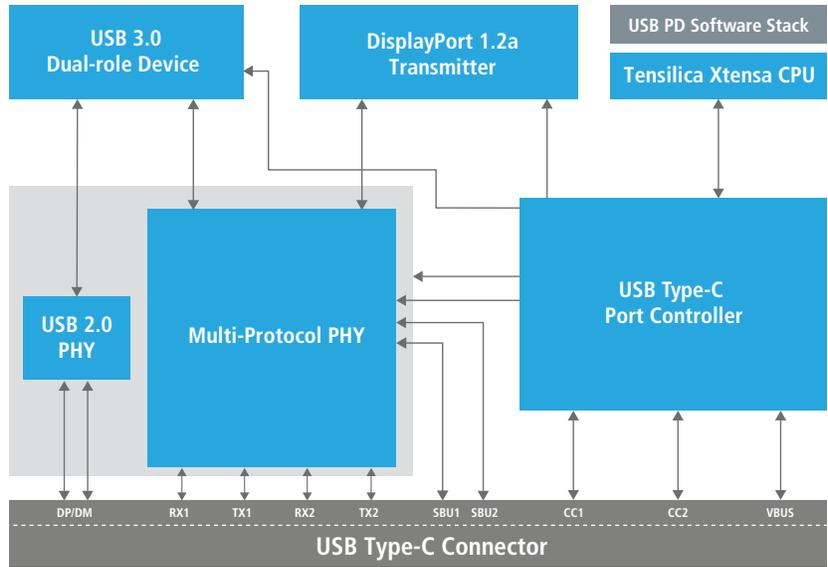


Figure 2. USB Type-C/DisplayPort IP subsystem

Summary

With USB Type-C poised to become a dominant connector specification for electronic devices, now is a prime opportunity to become familiar with the design considerations for USB Type-C as well as the USB Power Delivery 2.0 and USB Alt Mode specifications. Given the challenges, along with the cost and time sensitivities for the end products, especially in mobile applications, a USB Type-C IP subsystem presents a viable way to meet your performance, power, and time-to-market targets.

Footnotes

1. Ngo, Dong, "USB Type-C: One cable to connect them all," March 9, 2015, <http://www.cnet.com/news/usb-type-c-one-cable-to-connect-them-all/>