

Simulation VIP for MIPI I3C

Complies with MIPI I3C specification version 0.7

Overview

Cadence® Simulation VIP is the world’s most widely used VIP for digital simulation. Hundreds of customers have used Cadence VIP to verify thousands of designs, from IP blocks to full systems on chip (SoCs).

The Simulation VIP is ready-made for your environment, providing consistent results whether you are using Cadence Incisive®, Synopsys VCS®, or Mentor Questa® simulators. You have the freedom to build your testbench using any of these verification languages: SystemVerilog, e, Verilog, VHDL, or C/C++. Cadence Simulation VIP supports the Universal Verification Methodology (UVM) as well as legacy methodologies.

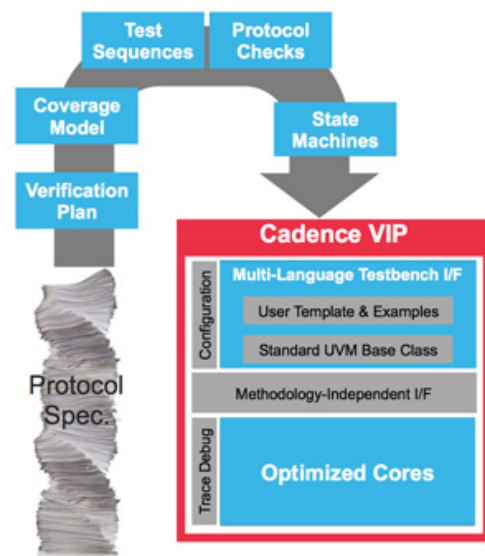
The unique flexible architecture of Cadence VIP makes this possible. It includes a multi-language testbench interface with full access to the source code to make it easy to integrate VIP with your testbench. Optimized cores for simulation and simulation-acceleration allow you to choose the verification approach that best meets your objectives.

Specification Support

The I3C VIP complies with MIPI I3C specification version 0.7 which is still under review by the MIPI Alliance Organization.

Supported Design-Under-Test Configurations

- | | | |
|--|---|-------------------------------------|
| <input checked="" type="checkbox"/> Master | <input checked="" type="checkbox"/> Slave | <input type="checkbox"/> Hub/Switch |
| <input checked="" type="checkbox"/> Full Stack | <input type="checkbox"/> Controller-only | <input type="checkbox"/> PHY-only |



Deliverables

People sometimes think of VIP as just a bus functional model (BFM) that responds to interface traffic. But SoC verification requires much more than just a BFM. Cadence Simulation VIP components deliver:

- State machine models incorporate the subtle features of state machine behavior, such as support for multi-tiered, power-saving modes
- Pre-programmed assertions that are built into the VIP to continuously watch simulation traffic to check for protocol violations.
- Test suites are provided for most Cadence VIP components.
- Pre-programmed coverage models used to capture interesting combinations of simulation results. By analyzing the results collected by the coverage model, engineers can tell if the simulations have exercised the various modes of operation of an interface.
- Verification plans for most protocols link the “raw” coverage model results back to the protocol specification.

Key Features

- Supports HDR-TSP and HDR-TSL modes.
- Supports processing Secondary Master mastership requests.
- Supports peer-to-peer slave data transmissions.
- Supports the mandatory dynamic address assignment mode including SETDASA.
- SDR private read/write data transfers.
- Supports optional 50 ns glitch filter for I2C devices.
- Sending of optional start byte in transactions is available.
- Supports Hot-join procedure for adding slaves to the bus on the fly.
- Supports processing of in-band Interrupts from I3C slaves.
- Supports I3C address arbitration.
- Mandatory and optional CCCs: Direct and broadcast commands.
- Implements user control of slave response fields such as data, slave busy, slave sending NACK, etc.
- HDR-DDR enter and exit patterns, command coding, bus turnaround and error detection.
- I2C Speed Modes: Fast, Fast Plus, Ultra Fast and High Speed

Test Suite

This VIP includes a basic test suite capability that includes:

- Constrained-random example tests
- 3rd party simulator test execution

Related Products

- MIPI CSI-2 Simulation VIP
- MIPI CSI-3 Simulation VIP
- MIPI C-PHY Simulation VIP
- MIPI -D-PHY Simulation VIP
- MIPI DigRF Simulation VIP
- MIPI DSI Simulation VIP
- MIPI LLI Simulation VIP
- MIPI M-PHY Simulation VIP
- MIPI SLIMbus Simulation VIP
- MIPI Soundwire Simulation VIP
- MIPI UniPro Simulation VIP
- MIPI CSI-2 Accelerated VIP
- MIPI DBI Accelerated VIP
- MIPI DSI Accelerated VIP
- UFS Memory Model



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