

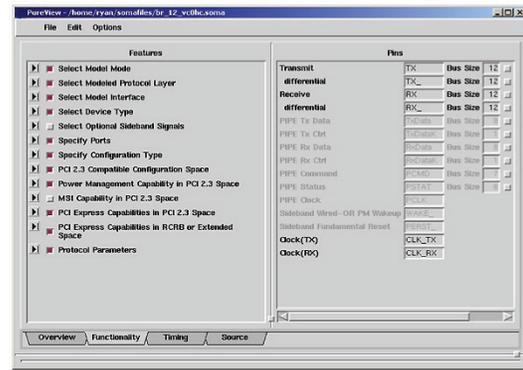
TripleCheck for MIPI CSI-2

Overview

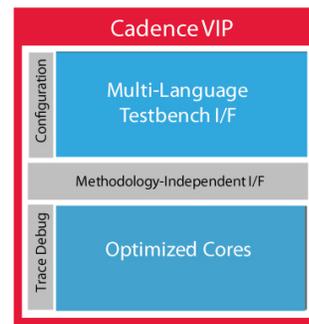
The Cadence MIPI CSI-2 TripleCheck VIP provides an easier way to ramp up quickly on your verification tasks. The vPlan helps to focus on a specific feature in the spec. When we combine that with the ability of the testsuite to reach nearly every vPlan item, we verify the design effectively, easily, and methodically. In addition, using TripleCheck helps the team to assess the project's progress by tracking the overall coverage grade week by week. The vPlan can be filtered based on the specified configuration which holds a set of parameters describing the DUT. A user can match the VPlan sections to the DUT capabilities, thus allowing the vPlan to automatically filter portions of the spec that are irrelevant to a particular design.

For some, it is important to reuse parts from an old environment. The vPlan's design allows users to incorporate the provided vPlan with the user's own vPlans. Moreover, the coverage model is not connected in any way to the testsuite, which means you can always run the legacy tests and collect coverage from those runs.

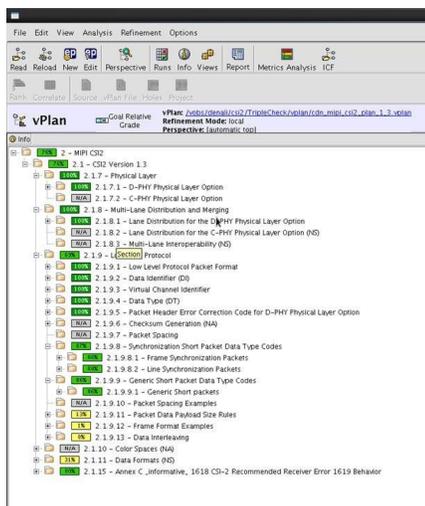
The combination of visualization that TripleCheck allows and the industry-proven CSI-2 VIP core offer a complete solution for teams where time is of the essence.



Configure



Run



Analyze

MIPI Features

Advanced Error Reporting: Stimuli and coverage collection of all applicable error scenarios

State Machines: Stimuli and coverage collection of all state machine transitions

Transaction formation rules: Stimuli and coverage collection of all applicable transactions

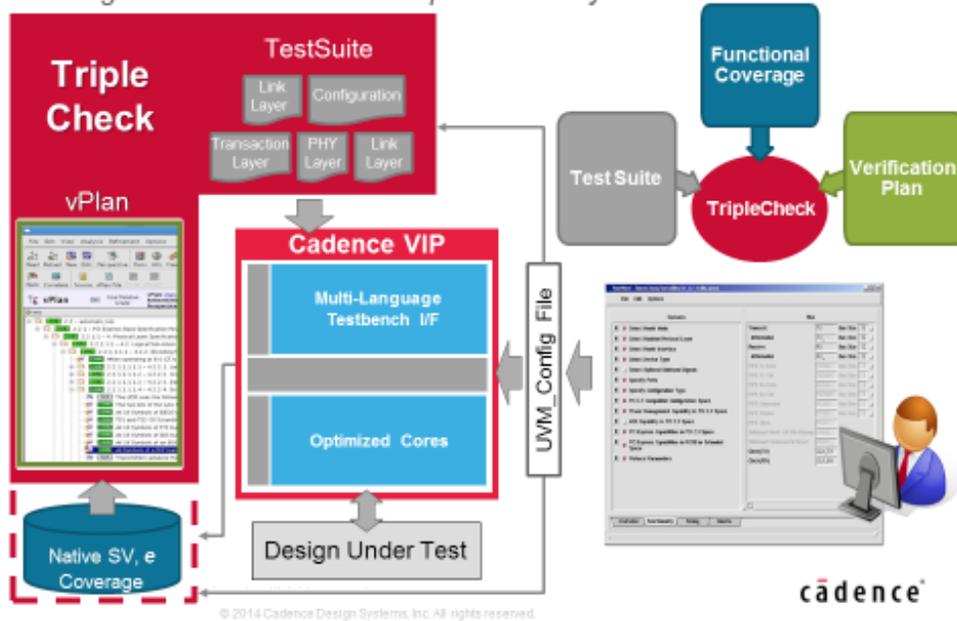
Physical Layer: 4 D-PHY data lanes CSI-2 receiver DUT

Multi lane distribution and merging: Distribution and merging of data between D-PHY data lanes.

Low level Protocol: CSI-2 frames and packet formats.

TripleCheck IP Validator

Third-generation interface compliance analysis



Test Suite

TripleCheck provides an extensive library of test sequences to stimulate the design under test. The test library contains directed tests (providing quick checks for common protocol compliance issues) as well as constrained-random test sequences for exhaustive testing to detect corner-case bugs hidden in the design. The tests support error injection in each layer of the protocol stack to check operation of the design when faced with non-compliant stimulus. This combination of directed and constrained-random tests results in high functional coverage, right out of the box.

Coverage Model

Coverage models are provided in both SystemVerilog and e verification languages. These pre-defined coverage models capture all data items and state machine transitions to track and measure verification progress. The coverage models are open and documented, which allows you to extend them with application-specific coverage definitions.

Verification Plan

TripleCheck provides a verification plan that mirrors the protocol specification. All the requirements in the protocol specification are listed in the plan and organized into the same chapter and paragraph hierarchy.

The vPlan is linked to the coverage model so that the coverage data captured during simulation runs is automatically mapped against the plan. This makes it easy to track verification progress and determine how much work remains. The vPlan is written in XML to enable portability between simulation environments.

In the Cadence® Incisive® simulation environment, TripleCheck integrates with the Incisive vManager tool to enable a number of productivity-boosting features, such as bucket analysis to analyze coverage details and test profiling to sort out unproductive test sequences.

Third-Generation Solution

TripleCheck is a third-generation pre-silicon compliance test suite solution. It combines the features from Cadence's other test suite solutions to deliver the most advanced pre-silicon compliance test suite on the market.



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