

# DDR2 Assertion-based VIP

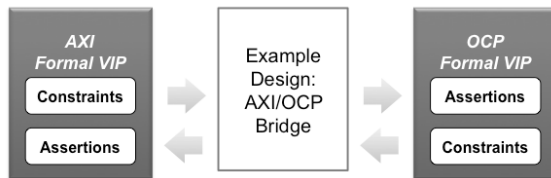
## Overview

Formal analysis is a mathematical approach to verification that has the unique ability to prove that a design is 100% correct. This method is tremendously useful, but is limited in the size and types of designs that can be verified. Still, for IP blocks with bus-style interfaces, it is an ideal verification solution.

Cadence® Assertion-Based VIP simplifies formal verification through its plug-and-play approach. Just attach the VIP to your design and run – no need for complicated tests and coverage analysis.

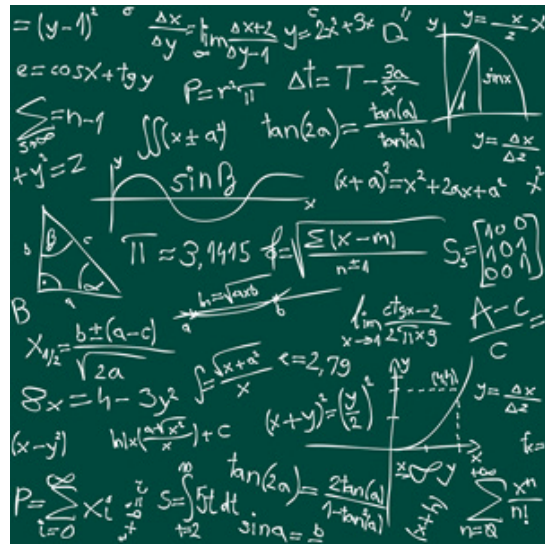
## No Tests Required

With Cadence Assertion-Based VIP, no test creation is required. Unlike logic simulation that uses test sequences to stimulate a design, a pre-programmed set of “constraints” is supplied with the assertion-based VIP. These constraints describe the range of all possible stimulus for a given interface specification. Also, “assertions” in the VIP check the interface signaling to make sure your design is acting in accordance with the protocol specification. You can start verifying your design in minutes with our assertion-based VIP.



## Debug Made Easy

Cadence Assertion-Based VIP works with the Cadence Incisive® Formal Verifier tool to make debug easy. When the VIP detects a design error, Incisive Formal Verifier displays a waveform trace, schematic view, and source code analysis of the bug. This makes it easy to find the root causes of bugs – and fix them!



## Specification Support

The DDR2 ABVIP supports the JEDEC Standard DDR2 SDRAM (JESD79-2F) protocol specification.

## Product Highlights

- Supports all legal data (DQ) and address widths configuration
- Supports all legal bank address widths configuration
- Supports configurable CKE minimum pulse width
- Supports different burst lengths of 4 or 8
- Supports all legal CAS latency
- Supports mode register set command
- Supports extended mode register command
- Supports all legal values of the auto precharge for each burst
- Supports different additive latency value

## Supported Design-Under-Test Configurations

- |  |   |                                     |
|--|---|-------------------------------------|
| <input checked="" type="checkbox"/> Master     | <input checked="" type="checkbox"/> Slave | <input type="checkbox"/> Hub/Switch |
| <input checked="" type="checkbox"/> Full Stack | <input type="checkbox"/> Controller-only  | <input type="checkbox"/> PHY-only   |