DDR Assertion-based VIP

Overview

Formal analysis is a mathematical approach to verification that has the unique ability to prove that a design is 100% correct. This method is tremendously useful, but is limited in the size and types of designs that can be verified. Still, for IP blocks with bus-style interfaces, it is an ideal verification solution.

Cadence® Assertion-Based VIP simplifies formal verification through its plug-and-play approach. Just attach the VIP to your design and run – no need for complicated tests and coverage analysis.

No Tests Required

With Cadence Assertion-Based VIP, no test creation is required. Unlike logic simulation that uses test sequences to stimulate a design, a pre-programmed set of “constraints” is supplied with the assertion-based VIP. These constraints describe the range of all possible stimulus for a given interface specification. Also, “assertions” in the VIP check the interface signaling to make sure your design is acting in accordance with the protocol specification. You can start verifying your design in minutes with our assertion-based VIP.

Specification Support

The DDR ABVIP supports the JEDEC DDR SDRAM STANDARD (JESD79F) protocol specification.

Product Highlights

- Supports all legal data (DQ) and address widths configuration
- Supports sending of data before address transactions
- Supports different burst lengths of 2, 4, or 8
- Supports all legal CAS latency
- Supports mode register set command
- Supports configurable auto refresh and self refresh mode
- Supports different period of active bank to another active bank

Supported Design-Under-Test Configurations

- [x] Master
- [x] Slave
- [ ] Hub/Switch
- [x] Full Stack
- [ ] Controller-only
- [ ] PHY-only

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