Overview

Verifying the standard interfaces in IP blocks and SoCs can be one of the most resource-intensive tasks for verification teams. Popular interface specification families such as ARM® AMBA®, DDR, MIPI, and others have undergone major expansions in recent years. Verification engineers seldom have more than a couple weeks to ramp up on a new protocol before they have to start verifying designs incorporating it. Commercial VIP helps offload part of the verification effort, but engineers still need a window into the protocol-specific interactions between the design, the VIP, and the testbench to find the root causes of bugs. Such a window is provided by the Indago Protocol Debug App, which presents a holistic picture of the verification environment in four views:

Channel Viewer
- Graphical presentation of transactions clarifies design behavior
- Select data types or packets to see preferred level of detail
- Error highlighting reveals design bugs

State Machine Viewer
- State machine diagrams relate design behavior to specification terminology
- See what states were visited during simulation
- View reasons for state changes and see event timing
- Drill down to lower-level state machines

Smart Log
- Set up multi-level queries to save and share
- Warnings and errors highlighted and connected to relevant packets

Life Story
- See everything that happened to a given object during simulation
- View registers, packets, state machines, lanes, queues configuration space, etc.
- Filter history to focus on important events
- Merge object histories from multiple simulations

Illuminate Design Behavior

The Channel Viewer portrays the communication between the design and VIP with a lab equipment-style view showing the sequence of transactions with protocol-specific labeling. The State Machine Viewer shows a graphical view of the state machines within the VIP components along with the causes of state transitions. The Life History and Smart Log provide detailed views of all events pertaining to simulation objects and smart filtering of messages. Together, these views present an integrated picture of the design and verification environment to simplify the debugging process.