

# Simulation VIP for MIPI DSI 2

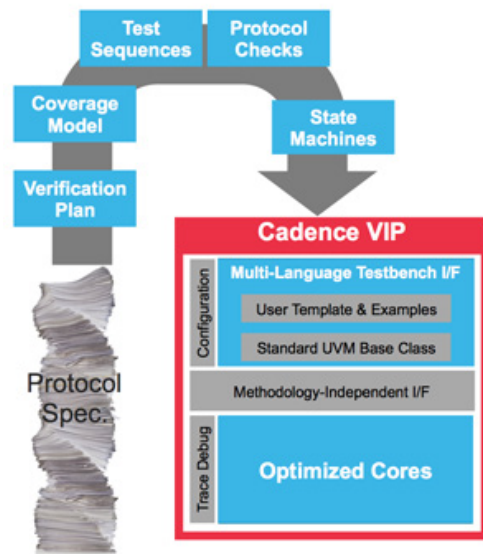
In production since 2008 on dozens of production designs

## Overview

Cadence® Simulation VIP is the world’s most widely used VIP for digital simulation. Hundreds of customers have used Cadence VIP to verify thousands of designs, from IP blocks to full systems on chip (SoCs).

The Simulation VIP is ready-made for your environment, providing consistent results whether you are using Cadence Incisive®, Synopsys VCS®, or Mentor Questa® simulators. You have the freedom to build your testbench using any of these verification languages: SystemVerilog, e, Verilog, VHDL, or C/C++. Cadence Simulation VIP supports the Universal Verification Methodology (UVM) as well as legacy methodologies.

The unique flexible architecture of Cadence VIP makes this possible. It includes a multi-language testbench interface with full access to the source code to make it easy to integrate VIP with your testbench. Optimized cores for simulation and simulation-acceleration allow you to choose the verification approach that best meets your objectives.



## Specification Support

The DSI-2 VIP supports the following MIPI specifications:

- MIPI DSI-2 specification, v. 1.0
- CPHY
- DPHY
- DBI
- DPI

## Supported Design-Under-Test Configurations

- |   |   |                                     |
|---|---|-------------------------------------|
| <input checked="" type="checkbox"/> Transmitter | <input checked="" type="checkbox"/> Receiver        | <input type="checkbox"/> Hub/Switch |
| <input checked="" type="checkbox"/> Full Stack  | <input checked="" type="checkbox"/> Controller-only | <input type="checkbox"/> PHY-only   |

## Deliverables

People sometimes think of VIP as just a bus functional model (BFM) that responds to interface traffic. But SoC verification requires much more than just a BFM. Cadence Simulation VIP components deliver:

- State machine models incorporate the subtle features of state machine behavior, such as support for multi-tiered, power-saving modes
- Pre-programmed assertions that are built into the VIP to continuously watch simulation traffic to check for protocol violations.
- Test suites are provided for most Cadence VIP components.
- Pre-programmed coverage models used to capture interesting combinations of simulation results. By analyzing the results collected by the coverage model, engineers can tell if the simulations have exercised the various modes of operation of an interface.
- Verification plans for most protocols link the “raw” coverage model results back to the protocol specification.

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## Key Features

- Verifies both DSI processor and peripheral.
- Supports both PHY interfaces (DpDn and PPI).
- Supports both High-Speed and Low Power data transmission.
- Supports several merged packets in a single PHY transmission.
- Supports both generation and checks of accurate video mode timings.
- Enables data scrambling in order to mitigate the effects of EMI and RF self-interference.
- Performs actual compression/decompression and provides set of checkers for monitoring of DSC-related traffic
- Includes the MIPI D-PHY/C-PHY VIP for physical layer verification.
- Supports one to four data lanes.
- Supports Ultra-Low Power mode (ULPM), triggers and LP data transmission.
- Supports sending and receiving of DSI packets and frames in command mode and all video modes.
- Enables the user to control the frame and packet payload.
- Enable the user to control the packets that are sent during BLLP periods in non-VACT lines
- Supports 8, 16 and 32 bit PPI HS data bus widths over D-PHY 2.0. Supports 16 and 32 PPI HS data bus widths over C-PHY

## Related Products

- MIPI C-PHY Simulation VIP
- MIPI DSI Simulation VIP (includes D-PHY, DPI, DBI)
- MIPI DSI Accelerated VIP



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