

# Processor IP Power Specifications: A Cautionary Tale

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Designers familiar with board-level design have developed an intuitive feel for packaged-processor power specifications: the processor draws a certain amount of power, give or take a percentage based on process variation and speed binning. When evaluating processor IP, however, this intuition fails because of variability in how factors that affect power specifications are used and documented.

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## Introduction

While a packaged processor’s measured power specifications must account for all of the circuitry in the package, processor IP power specifications are based on simulations—and processor IP vendors are free to use or not use a number of power-dissipating functions when reporting power numbers. Many factors can greatly affect the power specifications listed on the processor IP’s specification sheet, including the target fabrication technology (both lithography size and process), the cell library used, and the execution activity imposed on the processor during power simulation. Consequently, caution and judicious reading of the vendor data sheets are called for when comparing power numbers for competing processor IP.

Figure 1 shows a sample of what a processor IP’s data sheet may say (the actual power number is not provided). It is the footnote that is important—it describes the fabrication process, synthesis options, and, in this case, that the power specifications do not include the clock tree. All of this information—as well as additional information that is not included in the footnote—is critically important when comparing processors. Each type of information is examined in more detail below.

Power	0.XXmW/MHz <sup>1</sup>
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Footnote:

1. Based on 28nm TSMC HPC process. Includes local program and data memory. Power optimized synthesis. Does not include clock tree.

Figure 1: Power Specifications in a Sample Processor IP Data Sheet

## Process Technology

Each manufacturing process is tailored to have distinct characteristics, and thus parametric values vary. For example, processes are crafted to yield greater speeds, smaller gate sizes (more gates per area), and power reduction. The process technology listed in Figure 1 is for TSMC’s 28nm high-performance compact mobile computing (HPC) IC fabrication process. Compared with

TSMC's 28nm low-power (LP) process, the 28nm HPC process enables 10% smaller die size and more than 30% power reduction. Note that even at the same lithographic geometries, different IC fabrication processes (for example, general-purpose vs. high-speed or one manufacturer vs. another) can result in as much as a 50% difference in power dissipation.

To make accurate comparisons, you will need processor IP specifications for the same fabrication process. You must know both the lithographic geometry (e.g., 28nm, 40nm) and the process type (e.g., general-purpose, low-voltage, high-performance). If the numbers are not based on precisely the same process, then they are not comparable. Although rule-of-thumb conversion factors are available to translate from one process or process geometry to another, conversion factors insert yet another layer of uncertainty into the comparison.

### Synthesis Optimization Setting

The footnote in Figure 1 states that the power specifications were obtained by setting command-line switches in the logic-synthesis tool to produce a power-optimized design. Power optimization, however, is not the only command-line switch setting available—synthesis runs can also be optimized for area or for speed. Each optimization setting produces a netlist that consumes different amounts of power per clock cycle because each setting produces different amounts of logic. In fact, processor IP data sheets that list maximum clock rate, silicon area, and power dissipation specifications often show numbers based on different synthesis optimizations for each specified number so that the numbers look as good as possible.

In addition, other parameter settings can be relevant based on the specific process technology used, such as:

- Process-voltage-temperature (PVT) corner
- $V_{TH}$ —threshold voltage, e.g., for RVT/ULVT/LVT/HVT cells
- Gate length—libraries vary gate length to trade leakage power vs. speed values
- Track height, e.g., 12-track fast or 7-track ultra-dense library

If the data sheet doesn't explicitly state the synthesis optimization settings used to obtain a particular specification, you need to ask the vendor for that information. These synthesis settings greatly impact power-dissipation and power-leakage numbers.

### Circuit Omissions

Many IP vendors' specifications do not include the processor's clock tree, which is a critical omission because the clock tree includes the gates that operate at the processor's highest frequency. A processor's clock tree dissipates much of the operating power in a properly designed processor. Omitting the clock-tree's power dissipation from the processor's power specification can reduce the published dissipation number by 30% to 50%. However, it is not possible to fabricate the processor IP without a clock tree. Make sure when comparing the power specifications of two processors that the clock tree is not omitted from just one of them. Further, the inclusion or exclusion of memory also makes a substantial difference in power-dissipation numbers.

Notably, four additional key factors that greatly affect the processor's power-dissipation specification are often not addressed in the specifications, and should be considered during evaluation:

- Operating voltage
- Physical cell library used during synthesis
- Whether the power numbers are pre- or post-place-and-route
- Program code used to exercise the processor during power simulation

### Operating voltage

For example, at 45nm, processors can operate on supply voltages ranging from approximately 1.1V to 0.7V—a 3:2 difference in operating voltage with a similar difference in the operating-power range. Clearly, it is important to know the supply voltage used to obtain the power specification listed in the data sheet.

### Physical cell library

Combined with the operating voltage, the physical cell library used during synthesis can also make a big difference. Lower voltages reduce power but also reduce the maximum clock speed significantly. If the processor does not need to run near its maximum clock speed, lowering the voltage has the largest effect on dynamic power consumption.

When comparing the dynamic and leakage power specifications for processor IP synthesized for maximum operating frequency on high-performance and low-leakage manufacturing processes, the dynamic power/MHz drops considerably using the lower threshold voltage of the high-performance process. At the same time, the leakage power can increase over 2,000X in some cases (leakage power is constant—it does not scale with clock frequency). Processors manufactured with high-performance processes can achieve clock rates approximately 50% higher than the processors manufactured with low-leakage processes. Note that vendors typically show dynamic power values, and do not provide leakage power values.

### Pre- or post-placement and routing

An additional factor that helps determine a processor IP's power number is whether the power simulation is performed before or after placement and routing (P&R). Typically, placement and routing increases area by about 10% to 15%. The increased area translates into additional capacitance, which in turn increases the dynamic-power dissipation numbers.

### Program code used during simulation

One more detail remains: what is the processor doing while the power simulations run? Even the benchmark program being run during power simulation can influence the processor's power-dissipation specifications. If, for example, the program running during power simulation is a loop of NOPs, you would expect lower power numbers than if the processor exercised its function and load/store units.

No standardized power-benchmarking programs exist for processor IP. EEMBC, the industry's benchmark consortium ([www.eembc.org](http://www.eembc.org)), has developed a power benchmark for packaged processors called EnergyBench, but it requires a physical embodiment of the processor and cannot yet be applied to processor-IP simulations. The closest that the processor IP industry has come to a power-benchmarking program standard is Dhrystone version 2.1, a benchmarking favorite for people who compare processors.

## Cadence Tensilica Xtensa Processor

While some people think that all RISC processors deliver about the same performance per clock cycle, designers can get a significant performance improvement for each clock cycle by customizing the processor for a specific application.

A designer can add custom instructions to the base instruction set architecture (ISA) for the Cadence® Tensilica® Xtensa® customizable processor to significantly reduce the number of cycles required for tasks. As a result, the custom processor will be slightly larger and have a higher average power dissipation per clock cycle; but, as the cycle count reduction is proportionally more than the increase in area, the total energy consumed (power-per-cycle multiplied by total cycles) is substantially reduced.

Example: A 20% increase in power dissipated per clock cycle, offset by a 3X speed up in task execution, actually reduces energy consumption by 60%. This reduction in required task-execution cycles allows the system either to spend more time in a low-power sleep state, or to reduce the processor's clock frequency and operating voltage, leading to further reductions in both dynamic and leakage power.

## Conclusion

While designers find it difficult to constrain power numbers for processor IP to make fair comparisons, it is possible. To ensure a fair comparison, make sure you understand how all factors, including both the details in data sheet footnotes and whether any critical data has been omitted. For a valid comparison, ensure the quoted power specification numbers for the processor IP have as many similar parameters as possible and are in similar operating environments.

## Additional Information

For more information on the unique abilities and features of the Cadence Tensilica Xtensa processors, see [ip.cadence.com](http://ip.cadence.com).



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