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How Verification IP Can Minimize LPDDR4 PHY IP Verification Complexity

By YJ Patil, Cadence Design Systems

The market for mobile computing continues to grow, and along with it the demand for ever-faster devices with more features and functions and ever-longer operation on a single charge. These market forces have driven the development of next-generation DRAM: Low Power Double Data Rate 4 (LPDDR4). Released by JEDEC, LPDDR4, as compared to LPDDR3, doubles the memory throughput for mobile computing devices, such as smartphones, tablets, and ultra-thin notebooks, while preserving the same low power consumption profile.

LPDDR4 PHY intellectual property (IP) serves as a bridge between memory controllers and memories, making it easier to develop mobile system-on-chip (SoC) designs by addressing the complexity of interacting with high-speed multiplexed memory interfaces. However, verifying these design IP cores can be challenging, as the LPDDR4 specification continues to evolve. This paper takes a look at how verification IP (VIP) can help address concerns such as the huge coverage space, future-proofing, interoperability, and design cycle objectives.

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Introduction

Today's mobile SoCs are capable of integrating advanced functionality in a relatively efficient way. At the same time, they are also increasing the bandwidth requirements to external memory resources. In addition, mobile SoCs must continually support new features without an increase in power consumption or additional drain on battery life. These are some of the challenges that are driving chip designers toward LPDDR4 technology.

Using design IP in a mobile SoC design can make the process more efficient, providing building blocks that bring essential functionality to support end applications. High-quality IP reduces the risks associated with aggressive schedules and the high costs of SoC integration.

Of course, design IP cores have to be verified to meet end-user applications in the system context. Also, as specifications evolve, you need to ensure that your IP core can stand the test of time. With LPDDR4 PHY IP cores, in particular, interoperability across a variety of memory vendors and memory types is critical. So, too, is interoperability across a variety of applications as defined by the DDR PHY Interface (DFI) specification, which defines the interface protocol between the memory controller logic and PHY interfaces. As such, verifying your LPDDR4 PHY IP core can be a time-consuming and laborious process.

What type of verification methodology can help you achieve the productivity your team needs while also meeting your design complexity and project schedule requirements? Using our experience in launching new LPDDR4 PHY IP, we'll take a look at how VIP can be a time-saver in pre-silicon verification of design IP.

Overview of Key LPDDR4 PHY IP Features

As shown in Figure 1, a typical mobile SoC has to interact with the memory sub-system, a critical component for a rich user experience. However, the memory sub-system could be a bottleneck for high-throughput data processing. PHY IP provides a bridge between external memory and the memory controller.
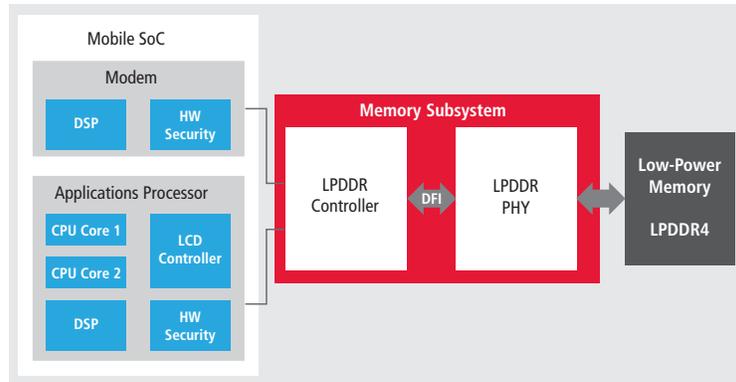

Figure 1: Mobile SoC design with LPDDR4 design IP

When it comes to LPDDR4 PHY IP, the implementation needs to be cost efficient, support an optimal balance between power, performance, and area, and meet all interoperability requirements. Figure 2 shows a block diagram of Cadence's LPDDR4 PHY IP core, which we will use as our use case highlighting how VIP can help minimize verification complexity. The Cadence® LPDDR4 PHY IP core supports DFI 4.0-compliant memory controllers and JEDEC JESD209-4-compliant memory devices. Its configurable slice-based architecture supports data widths beyond 64 bits, and it provides I/O throughput of 3,200 MTps. The core supports six DFI training modes, and supports rapid switching between frequency set points of LPDDR4 memory.
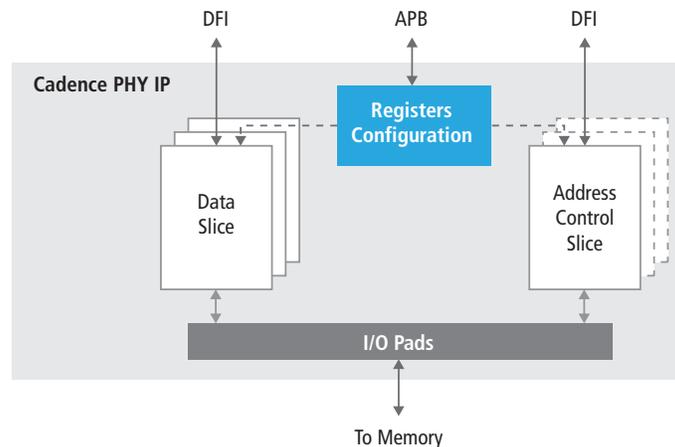

Figure 2: Cadence LPDDR4 PHY IP core

LPDDR4 PHY IP Verification Challenges

A variety of factors can turn design IP verification into a time-consuming and laborious process—one that can potentially impede the opportunity to meet the time-to-market window. On the implementation side, there are challenges related to the evolving specification and aggressive design schedules. There are also specification-related challenges, including the presence of:

• Complex interfaces with significant impact on overall system function

• Multiplexed interfaces with encoded commands to memory

• Several memory types and configurations

• Several training algorithms that need to be proven in the context of system design parameters

As a result of the above points, there's a huge functional coverage space to consider. Functional verification involves a cross of all of the features and parameters of each specification. Imagine the impact of crossing a 100-page JEDEC specification against an equally long DFI specification. The functional coverage space further grows as you configure your design to support multiple vendor-specific requirements based on clocking and power optimization needs.

One means to accomplish this verification process is to build and validate your own testbench to model your SoC's interfaces, a process that could take six months, and then test the design. VIP can streamline this entire effort. By modeling interfaces as components that you can then plug into an SoC testbench, pre-tested VIP can save months of time while also freeing up engineering resources to work on other aspects of the design project.

Overview of LPDDR4 VIP

As a key contributor to the JEDEC and DFI standards committees, Cadence has early insights that we've parlayed into robust implementations of VIP. Our LPDDR4 VIP implements JEDEC-compliant memories with all integrated checks. Figure 3 provides a PHY testbench diagram of DFI 4.0-compliant stimulus generation and checking enabled by a DFI Universal Verification Component (UVC) and Cadence verification IP (specifically, a DFI monitor).
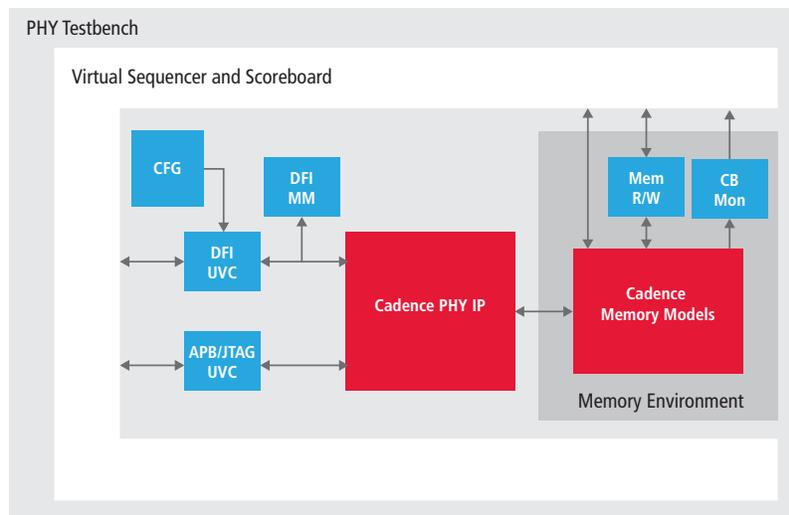

Figure 3: PHY testbench with DFI4.0 and LPDDR4 VIP

An external device modeled as part of the LPDDR4 VIP, LPDDR4 SDRAM is a high-speed synchronous DRAM device internally configured for two channels and 8-bank-per-channel memory with up to 16Gb density. It can be used to verify compliance to the LPDDR4 specification JESD209-4 and compatibility to memory vendor part models. Memory and timing parameters need to be modeled. The LPDDR4 model includes extensive timing checks, state machines (such as bank states, model state, and initialization status state), and memories (modeling LPDDR4 configuration states, configuration registers, and actual memory state). These features help to verify PHY design IP by generating warnings and errors when protocol or timing violations occur with respect to a dynamically changing model state.

Cadence's LPDDR4 VIP includes an LPDDR4 memory model and highly configurable, flexible simulation models. It provides support for integration with all popular verification environments with an API that is handled natively. The API includes facilities to exchange transactions and important notifications to scoreboards and monitors in a higher level verification environment, while managing its own suite of verification assertion checks and coverage. A SystemVerilog testbench would interface with the VIP through these API calls.

DFI VIP Monitor and Checker

The DFI protocol specifies the signals, timing parameters, and programmable parameters required to transfer control information between a memory controller and the PHY. There are two types of transactions on the DFI interface: PHY control transactions which cause some autonomous behavior in the PHY and memory transactions which get translated into transactions on the LPDDR4 SDRAM interface by the PHY. There can be multiple transactions occurring at any time, and multiple PHY control transactions can start in the same clock cycle. The complexity of signaling relationships as captured in the DFI specification needs to be accurately modeled and thoroughly tested before your design is ready.

The Cadence VIP validates compliance and compatibility of the DFI protocol. This VIP includes highly configurable and flexible simulation models of all the protocol layers, models, and packet types. It enables seamless integration of VIP into the verification environment, allowing verification teams to focus on developing the sequence library to test these features in their designs under test (DUTs).
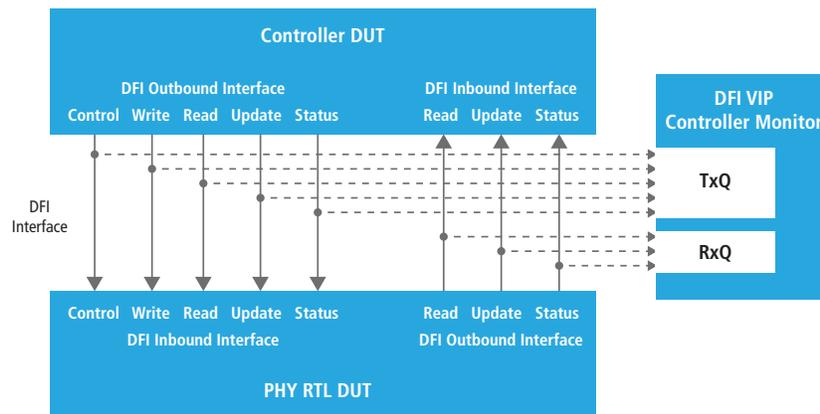

Figure 4: Cadence DFI VIP validates the compliance and compatibility of the DFI4.0 protocol.

Example: Verifying Rapid Switching Between Frequency Set Points of LPDDR4 Memory

LPDDR4 specifies two frequency set points (FSPs). According to JEDEC, these FSPs are copies of all the DRAM registers that store operating parameters that might need to be changed for operation at two different frequencies. Once both operating frequencies are trained and the parameters stored in each of the two corresponding FSPs, a single mode register write handles switching between the frequencies. This approach reduces the latency for frequency changes, and enables the system to operate at the optimal speed for the workload more often.

To support this feature from a DFI/SDRAM interface perspective, the PHY IP implements a shadow copy of the registers. Dynamic frequency scaling (DFS) feature testing calls for modeling of this behavior in the testbench, from stimulus, monitor, and scoreboard perspectives.

The LPDDR4 VIP implements "single mode register write to switch between frequencies", with no additional work required on the memory side. The testbench needs to implement shadow registers to seamlessly switch and predict correct operation. Bringing up the PHY from boot frequency, training memory at frequency-set one, and switching to the new training frequency entail a complicated test sequence that needs to be carefully crafted to avoid a long debug cycle. The ability to monitor to a full state of memory devices enabled by the memory model saves substantial time and debug effort.

Example: Verifying 6-Pin Single Data Rate Command Address Bus

For LPDDR4 devices, the goal is to time the command address (CA) bits [5:0] to have equal setup and hold times with respect to the rising edge of MEM CLK that occurs during the active CS. When the VALID CA value has equal setup/hold timing with respect to MEM CLK, this is considered "ideal" timing at the memory device, as shown in Figure 5.
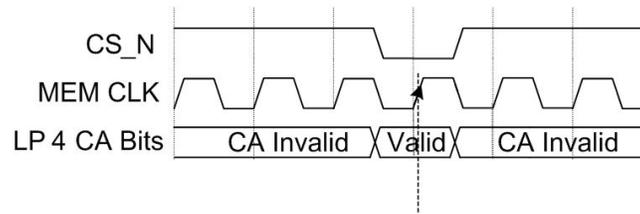

Figure 5: CA Training Ideal Timing

One CA training module is instantiated for each address slice module. Each CA training module works independently and in parallel to train their respective CA bits. A single CA-training response is formulated and sent back to the MC on the DFI bus. The CA slice in the PHY IP also contains a per-bit de-skewing capability, so any CA bits per module will be adjusted independently of each other. All CA bits will be trained independently, no matter which CA slice they belong to.

To be able to mimic the real-life scenarios of multiple CA modules, the testbench has to model and insert variable delays on the signal path. This is typically a time-consuming, error-prone exercise. The ability to introduce trace skew on each signal path and to control them is an important testbench feature. The LPDDR4 memory model provides the ability to build and seamlessly integrate custom logic. This enabled us to test and prove that the design is robust with various delay ranges. Using our LPDDR4 VIP, we accomplished our goal of stress testing the design IP against the specification. We also met the extended scope to test the design against potential issues stemming from the high-speed board design to minimize jitter.

Minimizing SoC Integration Risks

Cadence has performed extensive functional verification (pre-silicon) on our LPDDR4 PHY design IP:

• Proven design IP across JESD209-4 compliant memory models with full timing checks enabled

• Proven design IP across all supported memory vendor types with full timing checks enabled

• Proven design IP against DFI4.0 specification, full protocol compliance check with Cadence DFI monitor VIP

• Stress testing of per-bit-deskew for write and read data path

• Testing of complete sequence of training in different modes

• Exercising of Low Power Interface (LPI) feature

• Exercising of I/O calibration logic with SPICE simulations; model is proven against design IP

• Extensive testing of CA bus per-bit-deskew/flyby delay range/constraints

• Standalone functionality with SoC isolation, which means that the PHY is operational via JTAG interface, debug interface is tested

• Testing of scan support with BIST features

• Exercising of gate-level simulations with Standard Delay Format (SDF) delays

• 6000+ constraint random test seeds covering 2000+ functional coverage bins

• Rigorous signoff process to meet key customers' needs/flows

Summary

Design IP reuse is now pervasive across every segment of the semiconductor industry, especially for mobile SoCs. Memory bandwidth has always been a critical factor for the performance of many data-intensive applications. LPDDR4 PHY IP is an enabler of high-throughput transactions to memories; therefore, it's critical for PHY IP to operate reliably across various system design requirements. It is just not sufficient to only have PHY IP tested to ensure it meets the IP spec. Components that are used in this verification process also need to be extensively tested to ensure they model the interface spec. The whole effort is resource-intensive and error prone if left for a single IP verification team.

Cadence LPDDR4 PHY IP is verified using industry-standard verification IP cores, which are extensively tested (both with vendor models and for the full specification compliance), along with a robust testbench environment that was built by an experienced team to exercise the full specification. Cadence continues to evaluate additional methods, design, and verification techniques to keep ahead of the curve to enable high-speed/low-power memory IP cores to meet the evolving needs of mobile SoCs,

For Further Information

Learn more about Cadence LPDDR4 PHY IP at: http://ip.cadence.com/ipportfolio/ip-portfolio-overview/memory-ip/ddr-lpddr

Learn more about Cadence LPDDR4 verification IP at: http://ip.cadence.com/ipportfolio/verification-ip/memory-models/dram/lpddr4-memory-model

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