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Selecting an Optimized ADC for a Wireless AFE

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Today's wireless transceivers need to be small and consume as little power as possible, in order to support the myriad of smart, portable devices on the market. This paper examines two key architectures—pipeline and successive approximation register (SAR)—that are deemed suitable for the analog-to-digital converter (ADC) that is a key component of a wireless analog front end (AFE). The paper then discusses why the SAR architecture is the most ideal of the two to meet power and performance requirements at advanced nodes.

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Introduction

As more and more portable devices connect to the Internet, the need for power-efficient wireless transceivers is on the rise. Simultaneous proliferation of multiple wireless protocols necessitates flexible and configurable RF system design. As a consequence, RF system designers are today faced with the challenge of designing the most power-efficient, smallest yet configurable RF transceivers. Based on the frequency of operation, analog modules in an RF signal chain can be broadly classified as RF and baseband systems. This paper discusses the various trade-offs these modules offer and how best they can be optimized to achieve optimal performance in a cost-effective way.

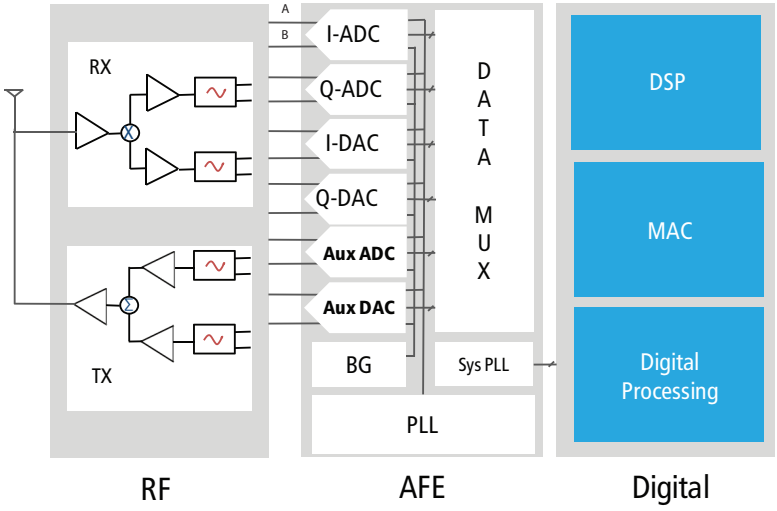

Figure 1. Simple complete RF signal chain

Figure 1 shows a simple complete RF signal chain. For the sake of simplicity, the system has been divided in three modules – RF, analog front end (AFE), and digital. This paper talks about system optimization for the first two blocks.

A Look at Wireless Protocols

A relaxed RF module would need a very stringent AFE and, at the same time, a very relaxed AFE would need an extremely complex RF block. As a protocol matures, a consensus is generally arrived for system partitioning between the RF and AFE. As of this year, there is a reasonable consensus for optimal partitioning for 802.11a/b/g/n and Long-Term Evolution (LTE). The specifications for RF and AFE modules have become fairly standard. However, as the new addition to the 802.11x family, 802.11ac/d, as well as LTE-Advanced (LTE-A) are increasingly adopted, ongoing system optimization is focused on these standards. LTE is the 4th generation (4G) wireless communication standard for high-speed mobile data transfer. The standard was proposed by the 3GPP consortium in their Release 8. It occupies a maximum channel bandwidth of 20MHz, and uses techniques like OFDM and MIMO to achieve peak data rates of 300Mbps. 802.11ac is the 5th generation WLAN standard belonging to the 802.11 series developed by IEEE, and supports a maximum data rate of 6.93Gbps.

Defining an RF System

When a system designer is ready to define an RF system, he or she usually starts with the protocols targeted. The specifications for an AFE are derived by RF system designers for a particular protocol. As data rates are set by a protocol, the system designer has limited flexibility to trade-off complexity of the design between the RF block and AFE IP.

The key parameter that decides the sampling rate of the analog-to-digital converter (ADC) is the bandwidth of the baseband signal. According to the Nyquist sampling theorem, to avoid any information loss during sampling, the sampling rate of an ADC must be more than twice the bandwidth of the baseband signal. This assumes a brick wall filtering by the RF stage to ensure that all the frequencies above the data rate have been eliminated. However, this is unrealistic. Some frequency components remain and, hence, more than twice the sampling rate is preferred. The safety margin is at the discretion of the designer.

The resolution/accuracy of the sampling is determined by the modulation scheme as a minimal signal-to-noise ratio to be ensured at the digital baseband for successful demodulation. Other factors, like receiver sensitivity, adjacent channel rejection, and noise figure, also play an important role in deciding SNDR of an ADC.

Specifying an ADC

In a typical implementation of a receive path, the ADC consumes the most power in an AFE. Power consumption has a direct relation with the battery life in a handheld device, so in order to increase the battery life for handheld devices, it is crucial to select an ADC with the lowest power consumption for given specifications. Quite a few ADC architectures have been found to be practical for earlier wireless standards. However, for the latest wireless standards, 802.11ac/d and LTE-Advanced, the major competition is between the pipeline and SAR architectures.

Pipeline vs. SAR Architecture

Pipeline architecture is a multi-stage conversion system where each stage quantizes the amplified quantization error signal from the previous stage, enabling higher throughput. However, due to its multi-stage architecture, it necessitates incorporation of a large number of precision analog building blocks, which increases its power consumption in advanced analog un-friendly process nodes. These features have worked against the pipeline architecture in advanced process nodes.

It was generally believed that the SAR architecture, in its classical form, would be unviable for higher speed and resolution as increases in resolution increase the size of the digital-to-analog converter (DAC) capacitor array exponentially. The SAR architecture also needs a higher frequency clock. However, some architecture enhancements and implementation techniques that split the capacitor array make it possible to optimize area for higher resolution. Advanced technology nodes offer power-efficient digital processing with reduced switching losses, by exploiting digital processing improvements offered by advanced nodes in analog-to-digital conversion. Today, the modified SAR architecture offers arguably the best speed-to-power ratio. SAR employs just one comparator; errors/non-idealities emancipating the comparator remain the same in all converted bits and, hence, are easier to correct.

These architectural advantages make SAR a clear winner between the two architectures for advanced process nodes.

Inside a SAR ADC

The basis of the SAR architecture is its binary search algorithm. In its purest form, the SAR ADC consists of fewer blocks – SAR logic, a comparator, and a DAC. The basic operation principal of SAR is well documented in the literature and is beyond the scope of this paper. In this section, we focus on the improvements from the classical SAR architecture that make it attractive for high-speed, high-resolution ADC implementations.

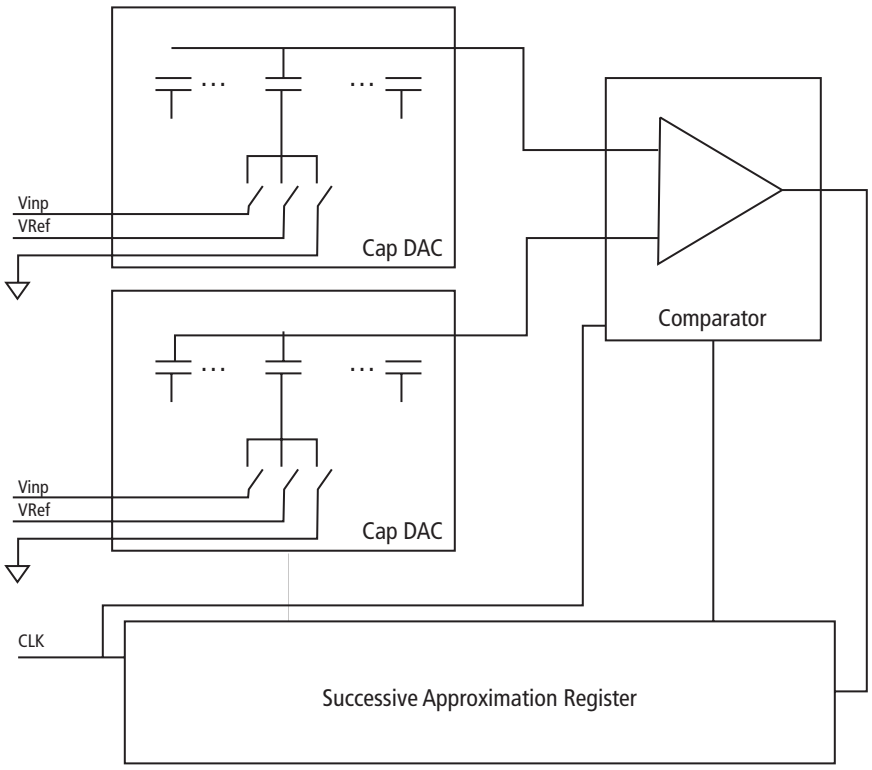

Figure 2. Typical implementation of a differential SAR ADC

Sample and Hold Circuit or Capacitor DAC

Figure 2 shows a typical implementation of differential SAR ADC. The input (or inputs for a differential ADC) in a SAR architecture is (are) fed to a sample/hold circuit. This circuit samples the input voltage and ensures that, during the comparison phase, the inputs to the comparator remain constant irrespective of the change in the input voltage. In a SAR ADC, a sample and hold amplifier (SHA), is generally implemented through a capacitor DAC.

Need for an Input Buffer in ADC of an AFE

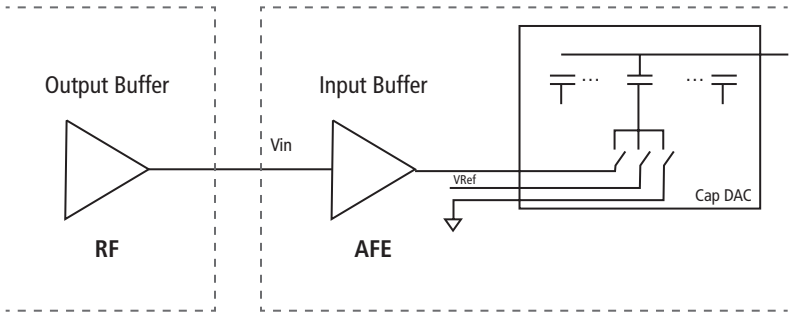

Figure 3. Input buffer in an RF system

Strictly speaking, an input buffer (Figure 3, shown in an RF system) is an optional component in an RF AFE. However, considering the advantages it offers, the input buffer has of late become a more regular, rather than an optional, component in an ADC. The input buffer eliminates any kick-back from the AFE block to RF section by ensuring high impedance to RF block and low impedance to ADC core. Additionally, it can be used to set the common mode of the ADC, irrespective of the common mode voltage of the output of the RF block. This feature provides great flexibility in selecting an RF module, as it enables interfacing the I/O voltage-supplied RF block to the core voltage-supplied ADC. Finally, the input buffer makes the design of the RF output buffer simpler as the former drives the "drain" of the switches, which offers varying capacitive load, and the latter just drives a DC load.

Power Consumption in a SAR ADC

In a high-speed SAR ADC that includes an input buffer, more often than not, the input buffer consumes power as much as the ADC core itself. An ultra-low power ADC core does not mean that, in system implementation, it will be the most optimal. In reality, such a low-power ADC needs an input buffer that takes the bulk of the power. So, while selecting an ADC for an AFE, it is essential to compare two "complete" ADCs and not just the core. Consider an example of a 12-bit, 160MSPS ADC. It converts an analog input in 6.25ns. In this duration, the input to the ADC core has to be stable and it has to convert its input to digital. If the ADC core settling time is 5ns, the input buffer will have settle its output at the accuracy of the ADC -- that is, 12 bits in 1.25ns! This will require an ultra-fast input buffer, which would be extremely power-hungry. So, in order to achieve low-power, high-speed performance, ADC designers need to optimize the ADC core and input buffer together by carefully budgeting the power between the input buffer and ADC core. It is also useful for system designers to compare the input buffer and ADC core performance together for correct power estimation.

Summary

As wireless protocols continue to evolve, RF systems need to be flexible and configurable. What's more, given that these systems support a large variety of portable, Web-enabled devices, they also need to be small and power-efficient. This paper examined architectures for ADCs, a critical component of the AFEs that are part of every RF system. Our conclusion is that the SAR architecture is best suited to meet power and performance requirements at advanced nodes.

Cadence offers a portfolio of more than 250 silicon-proven, hardened IP cores—including AFEs, ADCs, and DACs—that can be integrated into a wide range of system-on-chip (SoC) designs. The newest data converter IP cores are suited to 28nm designs, providing up to 10X faster conversion rates (up to 3GSPS) with up to 50% less power consumption and up to 40% smaller area requirements compared to competing IP solutions on the market. The cores are based on a parallel SAR architecture and support next-generation applications including WiGig.

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