Outline

- Why VIP ?
- UVM Environment
- vPlan
- Conclusion
Why VIP?

- How long to develop verification model?
- Is it trusted and robust?
- VIP ensures specification compliance
  - Mature
  - Assertion-based verification
  - Direct / random patterns
  - Multiple verification methodologies.
PCle PureSuite

- PCI-SIG compliance checklist
- Multiple device types
  - Root complex, endpoint, switch, bridge
- Multiple interfaces
  - Serial, PIPE, 8b parallel, 10b parallel
- Thousands of compliance patterns
  - Physical Layer (PL)
  - Data Link Layer (DL)
  - Transaction Layer (TL)
  - Configuration Space (CFG)
PCIe PureSuite (cont)

- Easy to adopt, and easy to select test cases
- Run for many and debug one by one
Easy to Debug by Different Logs

- **Trace file**
  - All events the model receives
  - Primary used by technical support

- **History file**
  - Details of VIP model

- **Transaction file**
  - Transactions by VIP model
LTSSM XML Format

- XML file describes actions for each test case.
- Assist in debugging failed test case.
Why UVM?

- An open resource of methodology for verification
- Coverage-driven verification
  - Constrained random tests
  - Self checking
  - Coverage collection
- Communicated with standard TLM interfaces
- Reusable verification components
Some helpful built-in commands
- `uvm_factory`, `uvm_component`, `uvm_phase`
- `uvm_objection`, etc.

Transactions dump
Viewing object information through Data Browser, Sequence Viewer, and Transaction Stripe Chart.
- Profiling for performance analysis
  - Call graph for function/task
  - Finding performance bottleneck
  - Reduce simulation time

<table>
<thead>
<tr>
<th>Cumm</th>
<th>Self</th>
<th>CG Node</th>
</tr>
</thead>
<tbody>
<tr>
<td>9.62% (3953/41090)</td>
<td>9.62% (3953/41090)</td>
<td>denaliMemTransaction.transGetInternal</td>
</tr>
<tr>
<td>19.16% (7873/41090)</td>
<td>9.43% (3873/41090)</td>
<td>denaliMemTransaction.new</td>
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<tr>
<td>6.89% (2931/41090)</td>
<td>4.51% (1853/41090)</td>
<td>uvm_object_string_pool:get</td>
</tr>
<tr>
<td>20.06% (8241/41090)</td>
<td>3.07% (1260/41090)</td>
<td>denaliMemCbFunc</td>
</tr>
<tr>
<td>39.53% (16244/41090)</td>
<td>2.75% (1128/41090)</td>
<td>regInst.readReg</td>
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<tr>
<td>2.38% (978/41090)</td>
<td>2.38% (978/41090)</td>
<td>uvm_event.new</td>
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<tr>
<td>2.55% (1847/41090)</td>
<td>0.97% (978/41090)</td>
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<tr>
<td>15.42% (10244/66519)</td>
<td>0.89% (2951/66519)</td>
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<tr>
<td>1.16% (227/19545)</td>
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<td>2.78% (543/19545)</td>
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<td>1.04% (203/19545)</td>
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<td>denMem_transGet</td>
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<tr>
<td>0.27% (91/19545)</td>
<td>0.12% (44/19545)</td>
<td>denaliMemCbFunc</td>
</tr>
</tbody>
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Summary:
- UVM Simulation with IES
- Profiling for performance analysis
  - Call graph for function/task
  - Finding performance bottleneck
  - Reduce simulation time
Unwanted Heap Growth

```
Profiled Intervals:

<table>
<thead>
<tr>
<th>#start</th>
<th>#stop</th>
</tr>
</thead>
<tbody>
<tr>
<td>[1] 28051496.831002 NS</td>
<td>to 28051497.831002 NS</td>
</tr>
</tbody>
</table>

Memory Usage - 25.3M program + 2653.6M data + 2.0M profile = 2661.0M total CPU Usage - 11.9s system + 8965.3s user = 8977.2s total (53.9% cpu)

Stream Counts | 7664 hits total

<table>
<thead>
<tr>
<th>#hits</th>
<th>#inst</th>
<th>name</th>
</tr>
</thead>
<tbody>
<tr>
<td>99.9</td>
<td>7660</td>
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Most Active Modules | behavioral |

<table>
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</thead>
<tbody>
<tr>
<td>50.0</td>
<td>4</td>
<td>Verilog: Object Name Resolution</td>
</tr>
<tr>
<td>37.5</td>
<td>3</td>
<td>outside engine</td>
</tr>
<tr>
<td>12.5</td>
<td>1</td>
<td>User Code</td>
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Stream Type Summary Counts | 7664 hits total

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<tbody>
<tr>
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<td>2</td>
<td>HDL C interface</td>
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<tr>
<td>0.0</td>
<td>1</td>
<td>Outside engine</td>
</tr>
<tr>
<td>0.0</td>
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<tbody>
<tr>
<td>[1] 28051490.831002 NS</td>
<td>to 28051491.831002 NS</td>
</tr>
</tbody>
</table>

Memory Usage - 25.3M program + 2614.9M data + 2.0M profile = 2642.3M total CPU Usage - 11.8s system + 8949.7s user = 8961.5s total (0.0% cpu)

Stream Counts | 8 hits total

<table>
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</thead>
<tbody>
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</table>
Unwanted Heap Growth (cont)

Unwanted Memory TLP cumulated
vPlan

- Metric-driven verification (MDV)
- Verification plan from the specification.
- Map the coverage model and data to the plan
**vPlan (cont)**

- Functional verification closure.
- Prevent redundant pattern.
Conclusion

- Solid VIP architecture
- Support multi languages, methodologies, tools
- Helpful information and tool for debugging
- Fast verification closure
- High confidence level of simulation result
The IP boutique
M31 Technology Corporation

Competitive IPs
- First BCK USB 2.0 PHY
- Robust USB 3.0 PHY
- UHS memory compiler / cell library

Quality Assurance
- Passes TSMC IP validation center program
- ISO9001:2008 certification
- MACH Family
- First BCK USB 3.0 PHY

Founded in Taiwan
- Named after the M31 galaxy
- Initial capital $12M
- Independent IP provider
- IP business only

IP Alliance Partner
- Multi-foundry IP provider
- Join TSMC IP alliance
- ULP memory compiler / cell library
- MIPI M-PHY / PCIe PHY / SATA PHY

Emerging IP Provider
- 2013 Emerging IP Provider Award by TSMC
- 40/55/90nm foundry sponsored IP provider
- 28/40/55nm USB 3.0 PHY provider
**M31 Spirit**

**Messier 31 or M31**, known as the Andromeda galaxy, is a double nucleus spiral galaxy approximately 2.25 million light-years from the earth and contains one trillion stars. It is the most distant deep-sky object that is visible to the naked eye.

We expect every IP that has been developed by M31 Technology Corporation to be just like the M31 galaxy, inspiring unlimited imagination and bringing us a bright future - a dream soon to be seen and recognized the whole world over.
To be the most trustworthy IP company in the semiconductor industry

The ever increasing demand of time-to-market and cost-reduction in IC design market prescribes the growing trend of IP business.

Many design companies and foundries aim to leverage Asian semiconductor supply chain infrastructure and eagerly need a professional IP supplier who knows the local culture, people, technology and real needs.
TSMC IP Alliance Partner

40+ IP Alliance Partners – including Soft-IP Partners

Open Innovation Platform™
# Main IP Products

<table>
<thead>
<tr>
<th>High-speed Interface</th>
<th>Memory Compiler</th>
<th>Cell Library</th>
</tr>
</thead>
<tbody>
<tr>
<td>USB 2.0/3.0 PHY</td>
<td>UHS/ULP SRAM</td>
<td>UHS Cell Library</td>
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<tr>
<td>BCK USB 2.0/3.0 PHY</td>
<td>Via ROM</td>
<td>UHD Cell Library</td>
</tr>
<tr>
<td>MIPI D-PHY / M-PHY</td>
<td>TCAM</td>
<td>General Cell Library</td>
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<tr>
<td>UniPro Controller</td>
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<tr>
<td>SATA 3 PHY</td>
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<td>MACH Optimization Flow</td>
</tr>
<tr>
<td>PCIe Gen 2/3 PHY</td>
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</tr>
<tr>
<td>USB 3.1 PHY</td>
<td></td>
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</tr>
</tbody>
</table>

**Fast-Monte-Carlo Analysis**
Target Application

16/28/40nm

AP
Mobile
TV
Tablet
Media Player

28/40/55nm

SSD
eMMC/SD
Pen-drive

More-than-moore

Smart-card
MCU
Power/Driver
## 2014-2016 IP Roadmap

### UniPro Controller/USB, PCIE, SATA controller-partner eco-system building

<table>
<thead>
<tr>
<th>Technology</th>
<th>2014-2016 Roadmap</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>55G USB 3.1 PHY (10G)</strong></td>
<td><strong>55G USB 3.0 PHY (5G)</strong></td>
</tr>
<tr>
<td><strong>PCle/SATA Combo PHY</strong></td>
<td><strong>MIPI M-PHY TX/RX (Gear-3)</strong></td>
</tr>
<tr>
<td><strong>USB 3.0 PHY</strong></td>
<td><strong>Ultra-low-Vcc-Min SRAM Compiler</strong></td>
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<tr>
<td><strong>7-T Library</strong></td>
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</tr>
</tbody>
</table>

- **Planned**
- **Developing**
- **Ready**

### Technological Enhancements

- **USB 3.0 PHY (1.8V/2.5V I/O)**
- **Ultra-low-Vcc-Min SRAM Compiler**
- **ULP SRAM Compiler**
- **UHS SRAM Compiler**
- **12-T MACH Library**
- **7-T Library**

- **PCIe Gen-3 PHY (8G)**
- **MIPI D-PHY TX/RX (1.5Gbps, 4-Lanes)**
- **MIPI M-PHY TX/RX (Gear-3)**
- **USB3.1 PHY**
- **Ultra-low-Vcc-Min SRAM Compiler**
- **ULP SRAM Compiler**
- **UHS SRAM Compiler**
- **12-T MACH Library**
- **7-T Library**

- **PCIe Gen-3 PHY (8G)**
- **MIPI M-PHY TX/RX (Gear-3)**
- **USB3.1 PHY**
- **Ultra-low-Vcc-Min SRAM Compiler**
- **ULP SRAM Compiler**
- **UHS SRAM Compiler**
- **12-T MACH Library**
- **7-T Library**

### Technology Nodes

- **55G**
- **40LP**
- **28LP/LP+**
- **28HPM/HPC**
- **16FF+**
Our Commitment

**Quality**
- Seamless with TSMC 9000 IP program
- Comprehensive QA and validation system
- Silicon proven with high-yield guarantee

**Service**
- Dedicated support from IP integration to tape-out
- Efficient and in-time service mechanism
- Hot-line ERP system

**Competitiveness**
- Long-term IP roadmap
- Competitive specification and features
- Technology innovation