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VIP Datasheet

Cadence Memory Model Overview

Overview

Memory is a major part of every electronic product. Every system on chip (SoC) contains embedded memories and must also interface with external memory components. The operation of these interfaces impacts both SoC functionality and performance, making memory interface verification a crucial step in the SoC development process.

Cadence® Memory Models are the gold standard for memory interface verification. Used by more than 500 customers, Cadence Memory Models provide support for 6,500 memories spanning 60 memory interface types and 85 memory manufacturers.

Vendor Certification

Cadence has close relationships with leading memory companies and industry standards organizations. Cadence memory models for commercial memory components are based on the manufacturer's datasheets and are then provided to the manufacturer for certification. This closed-loop quality control process means that you can trust your simulation results. Models for new external memory standards that do not yet have commercial component providers and models for internal memory standards are based upon the specifications provided by the controlling standards body, such as JEDEC, ONFi, and SD Association. Cadence works closely with our early-adopter customers to ensure the quality of these models.

3D Memory Leadership

3D technology is reshaping the memory landscape for virtually all types of electronic products. The driving force behind 3D is the fact that while processor performance has continued to increase in accordance with Moore's Law, memory performance has not. The performance limit imposed by memory is well known and is commonly referred to as the "memory wall". While the memory wall has seemed insurmountable for a number of years, new 3D memory technologies are now poised to tear down that wall. Cadence is in the vanguard of support for 3D memory technology with first-to-market models for Wide I/O, Hybrid Memory Cube (HMC), High Bandwidth Memory (HBM), and DDR4 3D Stacking (DDR4-3DS)

Memory Models

The models are ready-made for your environment, providing consistent results whether you are using Cadence Incisive®, Synopsys VCS®, or Mentor Questa® simulators. You have the freedom to build your testbench using any of these verification languages: SystemVerilog, e, Verilog, VHDL, or C/C++.

Memory Model Portfolio

The Memory Model Portfolio enables all the memory models shown in the table below. A single license enables multiple instances of all the models in a single simulation session. Multiple licenses are needed to enable multiple simultaneous simulation sessions.

PORTFOLIO	
Cellular SRAM	Compact Flash
DDR 1, 2, 3	DDR 2
DDR DIMM (DDR Dual Inline Memory Module)	DDR SDRAM
DDR Synchronous Graphics RAM	DDR Synchronous RAM
Delayline	DFI
Embedded SSRAM	Embedded SSRAM TI
eMMC 1.0, 2.0, 3.0, 4.4	Enhanced SDRAM
FCRAM (Fujitsu Consumer RAM)	FIFO
Flash (Basic)	Flash ONFi
Flash Toggle NAND	Flash Toggle NAND2
GDDR 2,3,4 (Graphics DDR)	LBA NAND (Logical Block Addressing NAND Flash)
LL DRAM: Low-Latency DRAM	LPDDR 1,2: Low-Power DDR
LR DIMM (Load-Reduced DIMM)	Memory Stick
MemStick Pro	NAND Flash
NOR FLASH Spansion	OneNAND Flash
PROM (Programmable ROM)	Pseudo Burst SRAM
QDR SRAM (Quad Data Rate SSRAM)	Rambus DRAM
Rambus Turbo Mode	Register File
RLDRAM 1,2,3 (Read-Reduced Latency DRAM)	Scratchpad
SD Card	SD Card 3.0
SDIO	Synchronous DRAM
Synchronous Mask ROM	Synchronous RAM NEC
Wide I/O	

DDR3 Memory Model

- Provides DDR functionality and timing check support for precharge, activate, read/write mode, register write, write leveling, ODT checks, power down, self refresh and initializations
- Supports multiple data widths and densities: x4 – x16 width; 500M – 8G density
- Supports multiple speed grades: 800, 1066, 1333, 1600
- Provides multiple vendor support: Micron, Elpida, Eorex, Hynix, Nanya, Samsung, and Winbond
- Supports multiple other functions such as: state machine and timing checks; DLL change and clock frequency changes; bank groups; write leveling; MPR read training; input data masking; drift read output delay and refresh

DDR4 Memory Model

- Supports 3DS level command decoding
- Supports 3DS Read/Write commands for 2H/4H/8H combinations
- Provides DDR functionality and timing check support for precharge, activate, read, write, mode register write, write leveling, ODT checks, power down, self refresh, and initializations
- Supports multiple data widths and densities: x4, x8, x16 width; 2Gb to 16Gb density
- Supports multiple speed grades: 1600, 1866, 2133
- Provides multiple vendor support: Micron, Hynix, Samsung
- Supports multiple other functions such as: state machine and timing checks; DLL change and clock frequency changes; bank groups; write leveling; MPR read training; input data masking; drift read output delay, and refresh

eMMC 4.5 Memory Model

- Provides register support for CID/CSD/OCR and Ext_CSD registers
- Supports eMMC command/response protocols
- Supports high-capacity negotiation for devices larger than 2GB
- Supports cache read/write operations
- Supports multiple other functions such as: state machine and timing checks; voltage range checking; context IDs; data tag mechanism; DDR timing; discard command; extended partition types; high-speed 200MHz mode; and others

eMMC 5.0 Memory Model

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Flash ONFi 3.0, 4.0 Memory Model

- Supports CE_n pin reduction that allows multiple devices to be connected to a single “chip enable”
- Supports all three interfaces: SDR/NV-DDR/NV-DDR2
- Supports multi-plane read/program/erase/copyback operations
- Supports multi-plane cache operations: read/program
- Supports multi-LUN operations for simultaneous read/program/erase

Flash Toggle NAND 2 Memory Model

- Provides on-die termination, ODT, support
- Supports differential DQS pins
- Supports differential rebar pins
- Supports multiple dies with shared CEbar
- Supports multiple other functions such as: four planes with two address bits per plane; two planes with writes to two pages each

High Bandwidth Memory (HBM) Memory Model

- Implements internal Wide I/O 2 state machine and performs specified timing checks
- 128-bit wide data bus. Pseudo channel mode with 64-bit data
- The model supports a wide range of device densities
- Differential clock and read/write strobes
- All bank, per-bank and self-refresh. Refresh timing check

Hybrid Memory Cube (HMC) Memory Model

- Clock recover: Necessary for serial data reception
- Scramble/de-scramble: Each lane data is scrambled per Flit using the seed
- Generation/reception of TS1: Necessary for identifying lane reversal and lane synchronization
- CRC generation/checking: To check data integrity of packets
- Transaction layer packets: Encoding/decoding packet header

LPDDR3 Memory Model

- Provides DDR functionality and timing check support for precharge, activate, read, write, mode register write, power down, deep power down, self refresh, initializations, and all related timing checks
- Supports multiple densities: 4Gb to 32Gb
- Supports on-die termination
- Supports partial array self-refresh and per-bank refresh
- Supports multiple other functions such as: write leveling; CA training, device temperature sensor adaptation

LPDDR4 Memory Model

- Provides DDR functionality and timing check support for precharge, activate, read, write, mode register write, power down, deep power down, self-refresh, initializations, and all related timing checks
- Supports multiple densities: 4Gb to 32Gb
- Supports speeds up to 2133 Mt/s
- Supports dual channels which can function independently
- Supports multiple other functions such as: data mask and data bus inversion; on-the-fly burst length; configurable preamble and postamble

LRDIMM Memory Model

- Provides configurable DIMM topologies for ranks and components
- Supports flyby delays: DIMM to DRAM (for UDIMM); RCD to DRAM (for RDIMM/LRDIMM)
- Supports address mirroring
- Supports ECC check bits
- Supports multiple other functions such as: core RCD forwarding logic; RCD control word writes; parity as well as multiple DRAM features

DDR4 LRDIMM Memory Model

- Provides configurable DIMM topologies: DIMM, RCD, DRAM
- Supports flyby delays: DIMM to RCD; RCD to DRAM
- Supports address mirroring
- Supports configurable DQ maps
- Supports multiple other functions such as: core RCD forwarding logic; RCD control word writes; and parity as well as multiple DRAM features

DRAM vs. NAND FLASH

Historically, one of the biggest growth drivers in the DRAM industry was the memory consumption in personal computing platforms. However, the definition of personal computing platforms has rapidly changed to be centered on mobile platforms as opposed to desktops and notebooks. In this new mobile world, the demand for DRAM memory has been affected because NAND Flash is being used in place of DRAM for the system memory requirements. The DRAM industry has reacted to these changes by finding growth in new, emerging areas like high-performance computing and high-performance networking.

As the unending appetite for more mobility continues, the marketplace continues to be subjected to a pace of replacement never previously experienced. As quickly as notebooks became desktop replacements, now tablets are cannibalizing the notebook market.

One side effect of this cannibalization is that average DRAM consumption per device is on a downward trend. Traditionally, notebooks have had a minimum 4GB standard DRAM memory configuration whereas tablets are typically 1-2GB. Although the growth in tablet unit sales partly offsets this reduction, it's not enough to fill the void completely,.

To ensure design success in such a volatile environment, comprehensive model support for current and new standards in both NAND Flash and DRAM are required to fully leverage performance and power improvements.

Flash PPN DDR Memory Model

- Supports low-power/normal-power async/DDR modes of device operation
- Supports CRC for data read/write in DDR mode
- Supports scratch pad memory
- Supports DQS/RE complimentary pns in DDR
- Provides support for clearing program error lists

SD Card 4.0 Memory Model

- Supports 2L-HD mode, half duplex, which doubles data throughput
- Supports PHY-link interface
- Supports data burst streaming, which allows multiple model instances to be connected using a ring connection
- Supports boot code loading
- Supports multiple other functions such as: data burst retry; low-power mode; and speed ranges A&B

UFS 2.0 Memory Model

- UTP layer - UPIUs: NOP IN, NOP OUT, Query Request/ Response, Task Management Request/ Response, Command, Response, Data Out, Data In
- UCS layer - SCSI commands: READ (6, 10, 16), WRITE (6, 10, 16), Inquiry, Report LUNs, Read Capacity (10, 16), Test Unit Ready, Verify, Start Stop Unit, Mode Sense, Request Sense, Security Protocol In, Security Protocol Out, Send Diagnostic, Read Buffer, Write Buffer, Pre-Fetch (10, 16), Synchronize Cache (10, 16)
- Boot functionality supported
- LUNS and W-LUNS supported
- Interleaving of commands supported
- Queue depth of over 32 commands
- C-port connection to device UniPro
- Direct C-port connection to Host UniPro
- Supported use cases: UFS stand alone (Transaction mode or using CPort signaling interface) and Full stack UFS (with UniPro+MPHY over DPDN serial interface or with UniPro only over RMMI interface)

Wide I/O Memory Model

- Supports state machine and timing checks
- Supports data width up to 128-bit, single data rate
- Supports wide range of device densities
- Supports differential CK and DQS for future DDR extensions
- Supports partial array self-refresh and per-bank refresh

Wide I/O 2 Memory Model

- Supports state machine and timing checks
- Supports 64-bit data bus width at double data rate
- Supports wide range of device densities
- Supports complimentary data strobe for every 16 data bits
- Supports partial array self-refresh and per-bank refresh; backdoor reads/writes; comprehensive assertion library; power-on initialization; trace debug and transaction and memory callbacks

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