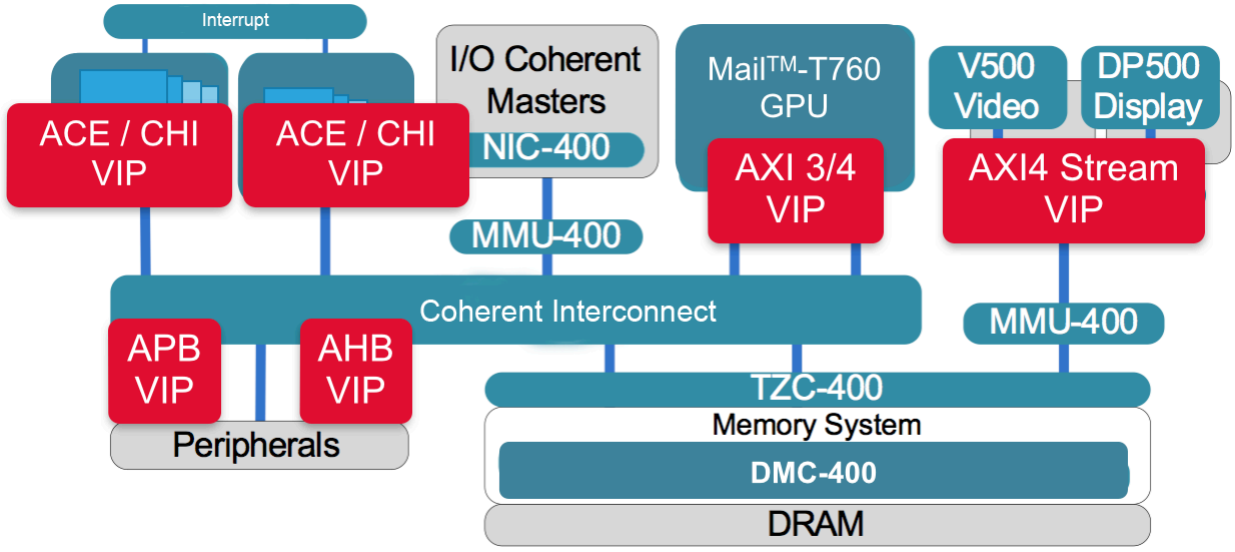
VIP Datasheet

Cadence VIP for AMBA Protocols

Overview

Cadence® VIP for AMBA Protocols helps you unleash your potential by offloading the tedious and error-prone aspects of functional verification. Proven on over 2000 projects, these VIP are trusted by engineers around the world. The solution includes Simulation VIP, Accelerated VIP, and Assertion-Based VIP to support logic simulation, hardware acceleration, and formal analysis. With Cadence VIP for AMBA Protocols, you'll have the power to get your job done right the first time.



A Three Pronged Approach For Best Results

To enable complete SoC fabric verification, three components are needed:

- Protocol compliance verification
- Data integrity analysis
- Performance verification

Protocol compliance checking is performed by the Simulation VIP, Accelerated VIP, and Assertion-Based VIP. Data integrity is verified with the Interconnect Validator, a unique VIP component that monitors all the transactions that flow across an interconnect to verify conformance to data transformation and cache coherency rules. Performance verification entails measuring bandwidth and latency results for simulated traffic. All three are part of the Cadence interconnect verification solution.

Protocol Compliance

Simulation VIP

The Simulation VIP is ready-made for your environment, providing consistent results whether you are using Cadence Incisive®, Synopsys VCS®, or Mentor Questa® simulators. You have the freedom to build your testbench using any of these verification languages: SystemVerilog, e, Verilog, VHDL, or C/C++. Cadence Simulation VIP supports the Universal Verification Methodology (UVM) as well as legacy methodologies.

AMBA 5 CHI Simulation VIP

- Supports link, network and protocol layer communication, including flow control mechanisms, across all RnX-to-HnX and HnX-to-SnX links
- Models the cache in RnF-to-HnF link
- Each link can take the part of either node as an active agent generating requests/snoops and responding according to the requests sent its way, or as a passive agent monitoring protocol correctness and collecting functional coverage
- Supports monitoring and driving of all protocol Opcodes, including barrier, exclusive access, and DVM.
- Active HN-F, which generates snoop requests and response to RN-F commands (when interconnect is not present).
- Supports link, network and protocol layer communication
- Support for Rn-F/Rn-D/Rn-I to Hn-F/Hn-D/Hn-I/Mn and Hn-F/Hn-I/Mn to Sn-F/Sn-I
- Available across all RnX-to-HnX and HnX-to-SnX links
- Users can delay the driving of each protocol flit.
- Facilitates the role of actual cache used in an CHI RN.
- Insert-specific or random values can be sent to the cache at the beginning of a test or during run time.

AMBA 4 ACE Simulation VIP

- The first and most widely used ACE VIP
- Includes support for AXI 4, AXI 3, and APB
- Allows ACE Lite configuration; automatically modify the agent accordingly
- Supports all legal data and address widths
- Supports the entire AXI spec. All AXI transactions can be sent and monitored
- Configurable option to use automatic slave responses
- Supports monitoring and driving of barrier transactions
- Cache model in both active and passive agents including cache state checks
- Supports controlling order in channels
- Supports sending of data before address transactions when legal
- Sets the delay between the items on the channels
- Supports monitoring and driving of DVM transactions
- Supports monitoring and driving of all exclusive transactions
- Supports monitoring and driving of locked transactions
- Supports both LPI controller and LIP peripheral agents
- Determines the values of the signals in the read and write address channel
- Determines the values of the signals in the write data channel
- Determines the values of the signals in the snoop response channel
- Determines the values of the signals in the snoop address channel
- Can support any number of agents
- Supports read-only and write-only interfaces
- Determines the values of the signals in the read data channel
- Supports connection to a snoop filter
- Supports monitoring and driving of all read and write transactions

AMBA 4 Stream Simulation VIP

- Customizable address and data width up to 32 bits
- Order in the interface is fully controllable by the user
- Sets the delay between the items on the interface
- Sets the delay between the items on the interface
- Determines the values of the signals in the write data channel
- Can support any number of agents

AMBA AHB Simulation VIP

- Supports all legal data and address widths
- Configurable option to use automatic slave responses
- Sets the delay between the items on the channels
- Determines the values of the signals in the read and write address channel
- Determines the values of the signals in the write data channel
- Memory can be set using backdoor access
- Can support any number of agents
- Easy testing of error scenarios
- Determines the values of the signals in the read data channel
- Supports slave memory emulation
- Supports monitoring and driving of all read and write transactions
- Configurable tracking of all the transactions on the channels
- Support for Hunalign and Hstrb
- Supports OKAY, ERROR, SPLIT, and RETRY
- Support retraction as defined in cortex M3 spec

AMBA AXI Simulation VIP

- The most widely used AXI VIP
- Includes support for APB
- Supports all legal data and address widths
- Supports AxQOS, AxREGION, and user-defined signals
- Allows AXI4 Lite configuration; automatically modifies the agent accordingly
- Configurable option to use automatic slave responses
- Supports controlling order in channels
- Supports sending of data before address transactions when legal
- Sets the delay between the items on the channels
- Supports monitoring and driving of all exclusive transactions

- Supports monitoring and driving of locked transactions
- Supports both LPI controller and LIP peripheral agents
- Determine the values of the signals in the read and write address channel
- Determines the values of the signals in the write data channel
- Can support any number of agents
- Supports read-only and write-only interfaces
- Determines the values of the signals in the read data channel
- Supports monitoring and driving of all read and write transactions

Accelerated VIP

Simulating big designs requires hardware-assisted verification, an approach that uses special-purpose hardware, like Cadence Palladium® XP systems, to dramatically boost simulation performance.

Just as simulation VIP simplifies traditional logic simulation, accelerated VIP makes hardware-assisted verification easier and more productive.

These accelerated VIP support simulation acceleration. In simulation acceleration, the Cadence Palladium XP system works in conjunction with the Cadence Incisive® Simulator to divide up the simulation task. The Palladium XP runs the design under test while the Incisive simulator runs the testbench. Accelerated VIP is inserted for each of the standard interfaces in the design with the testbench interface running on Incisive and the acceleration-optimized core running on the Palladium XP.

AMBA 4 ACE Accelerated VIP

- Generate and drive bus traffic as an ACE master
- Respond to bus traffic as an ACE slave
- The VIP supports all types of ACE transactions, including:
  - Barrier transactions
  - Cache maintenance transactions
  - Distributed Virtual Memory (DVM) transactions
  - Snoop transactions

AMBA AXI Accelerated VIP

- Generate and drive bus traffic as an AXI™ master
- Respond to bus traffic as an AXI slave
- The AXI AVIP supports all types of AXI transactions, including:
  –Unaligned transfers
  –Narrow transfers
  –Interleaved transactions
  –Outstanding transactions
  –Receipt of out-of-order transactions

AMBA AHB Accelerated VIP

- Generate and drive bus traffic as an AHB™ master
- Respond to bus traffic as an AHB slave
- Support batching mode in AHB master
- Support data bus widths of 32, 64, and 128 bits
- The VIP supports all types of AHB transactions
  –Narrow transfers
  –Outstanding transactions

AMBA APB Accelerated VIP

- Generate and drive bus traffic as an APB master
- Respond to bus traffic as an APB slave
- Support batching mode in APB master

Assertion-Based VIP

Cadence Assertion-Based VIP simplifies formal verification through its plug-and-play approach. Just attach the VIP to your design and run – no need for complicated tests and coverage analysis.

AMBA ACE Assertion-Based VIP

- Supports AXI4 and ACE protocols
- Provides comprehensive protocol compliance checking for the AXI™ cache coherency extensions (ACE)
- Features debug capabilities including AXI4- and ACE-specific transaction view

AMBA AHB Assertion-Based VIP

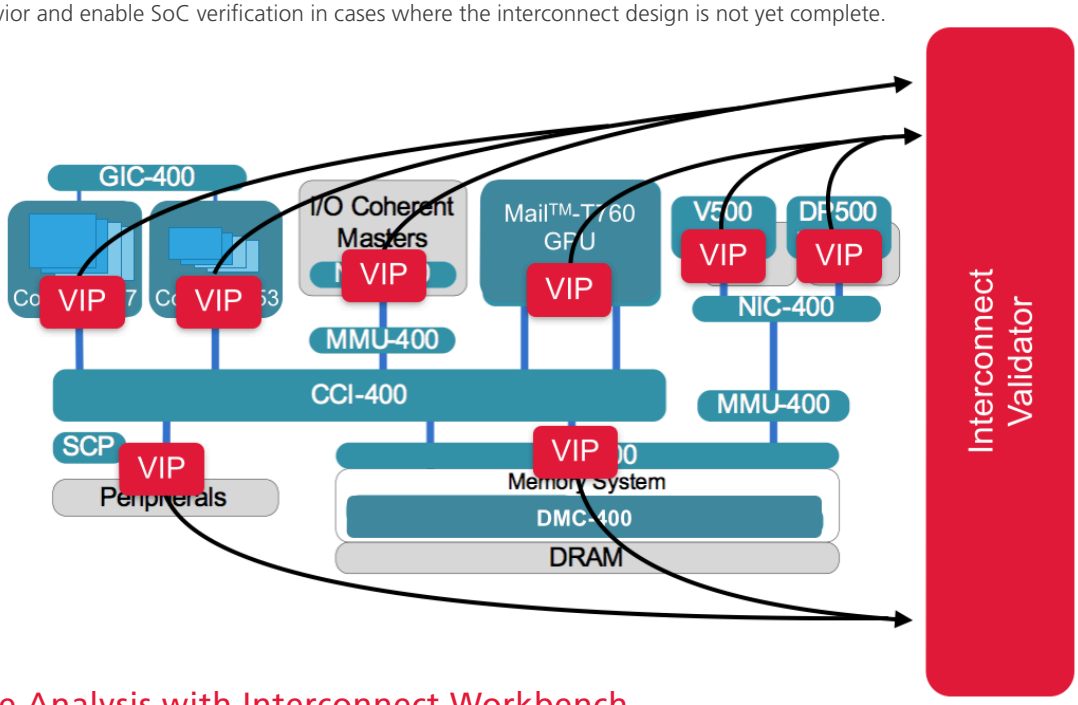
- Allows AHB-Lite configuration
- Supports round-robin or user priority based arbitration
- Supports burst reconstruction after split or a retry response, in addition to early burst termination
- Allows master to continue after error response
- Controls maximum length of INCR burst transfer
- Supports monitoring and driving of locked transactions
- Controls the burst type supported by master and the response type supported by slave

AMBA AXI Assertion-Based VIP

- Supports all legal data and address widths
- Supports sending of data before address transactions
- Supports interleaving of read/write data, wherever applicable
- Supports monitoring and driving of all exclusive transactions
- Supports monitoring and driving of locked transactions
- Supports low-power interface

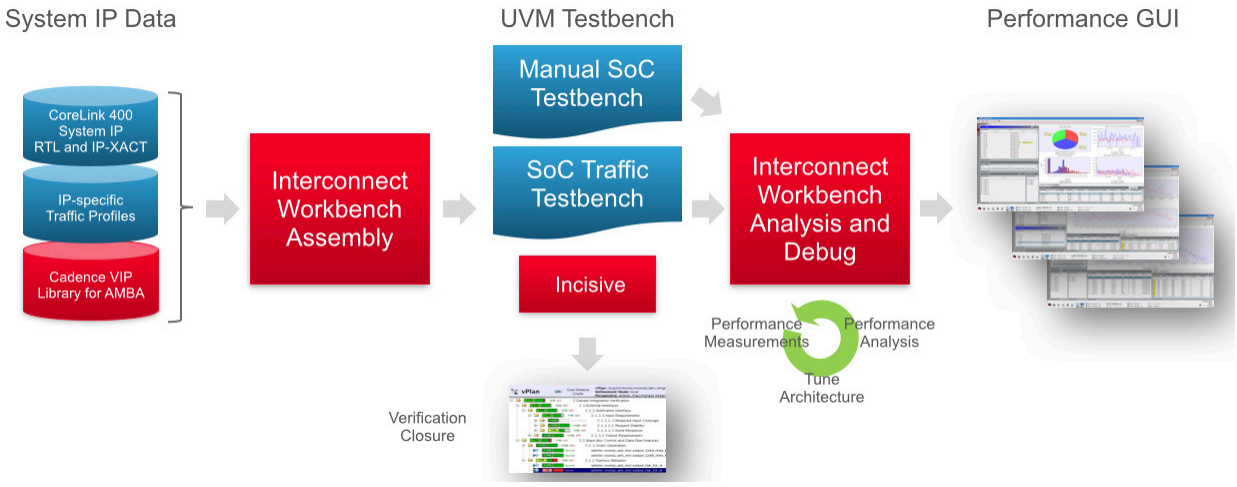
Data Integrity Analysis with Interconnect Validator

Cadence Interconnect Validator verifies the correctness and completeness of data as it passes through the SoC interconnect fabric. Because it automates a critical, yet difficult and time-consuming task, Interconnect Validator greatly increases your productivity. Interconnect Validator reduces verification effort by automatically creating a coverage model of all transactions exchanged between masters and slaves within an SoC. It includes a passive agent to monitor the SoC interconnect as well as an active agent to model interconnect behavior and enable SoC verification in cases where the interconnect design is not yet complete.



Performance Analysis with Interconnect Workbench

Your interconnect sub-system might be functionally correct, but are you starving your IP blocks of the bandwidth they need? Is the data from latency-critical blocks getting through on time? With the Cadence Interconnect Workbench, answering these questions becomes much easier. The solution collects cycle-accurate traffic from multiple simulation runs and displays latency and bandwidth measurements in an easy-to-use performance cockpit.



cadence

Cadence Design Systems enables global electronic design innovation and plays an essential role in the creation of today's electronics. Customers use Cadence software, hardware, IP, and expertise to design and verify today's mobile, cloud, and connectivity applications. www.cadence.com