Overview

Cadence® IP Factory delivers custom, synthesizable IP to support specific design requirements.

The Cadence Low-Jitter Integer Phase-Locked Loop IP is a clock multiplying integer PLL that supports a wide input frequency range and a VCO range from 600MHz to as high as 2200MHz, depending on the chosen IP and its process node.

This wide range of VCO frequencies combined with several programmable output dividers makes the Cadence Low-Jitter Integer Phase-Locked Loop IP versatile in supporting a wide range of input and output frequencies.

The Cadence Low-Jitter Integer Phase-Locked Loop IP is designed to generate analog sampling frequencies at a low accumulated rms jitter, which makes it ideal for SoC clocking applications. Its low period-jitter makes it suitable for systems implementing high-speed data-transfers.

Being silicon proven and having been extensively validated, the Cadence Low-Jitter Integer Phase-Locked Loop IP has a low die area and is characterized by low power consumption. This solution supports input frequency bypass options at the output, with a glitch-free transition being ensured from bypass to normal output clock.

Cadence IP Factory offers comprehensive IP solutions that are in volume production, and have been successfully implemented in more than 400 applications.

Key Features

- Low accumulated jitter PLL, suitable for analog sampling applications
- Low period-jitter, wide VCO frequency range
- Glitch-free transition from bypass to normal output clock ensured
- Input frequency bypass options at the output supported
- Programmable output dividers for wide frequency range support
- Flexibility in input and output frequency combinations

Figure 1: Example System-Level Block Diagram
Product Details

The Cadence Low-Jitter Integer Phase-Locked Loop IP is a low accumulated jitter phase locked loop that can be used to generate clocks for multiple standards and supporting multiple input and output frequencies.

Voltage controlled oscillator (VCO)

The VCO has an wide output frequency range from 600MHz up to 2200 MHz, depending on the particular process node choosen.

Charge pump

The charge pump has very good gain-linearity and very low static phase offset.

Output divider

There are six low power and high speed output dividers. Five dividers can be programmed using a 10-bit control word and one divider be programmed using a 14-bit control word. The division value is equal to (programmed value + 1).

Modes of operation

The Cadence Low-Jitter Integer Phase-Locked Loop IP can operate in three modes: active, power down and bypass.

The active mode is the normal mode of operation, while in the powerdown mode the device is powered down and consumes even less than 10µW, depending on the chosen process node. In the last one of the mentioned modes, the Cadence Low-Jitter Integer Phase-Locked Loop IP is bypassed and the output dividers will run at reference input frequency rather than VCO frequency.

Loop filter

Loop filter is fully integrated and controls the bandwidth and stability of the loop.

Cadence IP Factory

Cadence IP Factory can deliver various configurations of Analog IP to meet your design requirements.

For more information, visit ip.cadence.com

Available Products

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Process</th>
<th>Input frequency (MHz)</th>
<th>VCO frequency (MHz)</th>
<th>Core supply voltage (V)</th>
<th>I/O supply voltage (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>IP9239C</td>
<td>GF 28SLP</td>
<td>13 – 500</td>
<td>600 – 1600</td>
<td>0.93 – 1.07</td>
<td>1.62 – 1.98</td>
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<tr>
<td>IP9240C</td>
<td>TSMC 65LP</td>
<td>38.4, 40</td>
<td>600 – 1400</td>
<td>1.08 – 1.32</td>
<td>2.25 – 2.75</td>
</tr>
<tr>
<td>IP9242C</td>
<td>GF 65LPE</td>
<td>13 – 40</td>
<td>1600 – 2200</td>
<td>1.08 – 1.32</td>
<td>2.25 – 3.6</td>
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<tr>
<td>IP9243C</td>
<td>GF 55LPE</td>
<td>13 – 40</td>
<td>1600 – 2200</td>
<td>1.08 – 1.32</td>
<td>2.25 – 2.75</td>
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<tr>
<td>IP9244C</td>
<td>TSMC 40</td>
<td>13 – 40</td>
<td>1600 – 2200</td>
<td>1.05 – 1.16</td>
<td>2.25 – 2.75</td>
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<tr>
<td>IP9245C</td>
<td>TSMC 65LP</td>
<td>13 – 40</td>
<td>1600 – 2200</td>
<td>1.14 – 1.26</td>
<td>3 – 3.6</td>
</tr>
</tbody>
</table>

Benefits

• Wide operating range—wide range of input and output frequencies
• Low-power—power down and bypass modes supported
• Versatile solution—ideal for generating clocks for multiple standards

Deliverables

• FE views—Layout exchange format (LEF), .lib file, Verilog
• GDSII, netlist (SPICE format for Cadence Assura® Layout vs. Schematic Verifier (LVS))
• Footprint (LEF)
• User documentation, integration guidelines, engineering datasheet
• Silicon validation report (where available)

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