Overview

Cadence® IP Factory delivers custom, synthesizable IP to support specific design requirements.

The Cadence Low-jitter Fractional-N Phase-Locked Loop IP is a versatile clock multiplying PLL that supports a very wide input frequency range with the ability to generate VCO frequencies that are non-integer multiples of the input frequency.

The wide range of VCO frequencies, from 1000MHz to 2000MHz, combined with four programmable output dividers makes the Cadence Low-jitter Fractional-N Phase-Locked Loop IP versatile in supporting a wide range of input and output frequencies.

With low accumulated jitter in fractional mode and very low accumulated jitter in integer mode, the Cadence Low-jitter Fractional-N Phase-Locked Loop IP is an ideal frequency synthesizer for high-performance wireless and mobile systems.

The Cadence Low-Jitter Fractional-N Phase-Locked Loop IP is silicon-proven and has been extensively validated.

Cadence IP Factory offers comprehensive IP solutions that are in volume production, and have been successfully implemented in more than 400 applications.

Key Features

- High VCO frequency of 1000 – 2000MHz
- Low-power operation and a small die area
- Low RMS accumulated jitter and 27-bit fractional feedback division accuracy
- Supports a wide range of input crystal frequencies from 1MHz – 500MHz
- Four independently programmable output dividers for wide frequency range support
- Widely programmable output frequency range from 1MHz – 2000MHz
Product Details

The **Cadence Low-jitter Fractional-N Phase-Locked Loop IP** is a self-contained fractional mode PLL that accepts many standard crystal frequencies as the reference frequency and generates various VCO frequencies that can be divided to generate clocks for the analog front end as well as clocks for the digital sections of system-on-chip (SoC).

Jitter Values

The **Cadence Low-jitter Fractional-N Phase-Locked Loop IP** has a very low accumulated jitter of 6ps in integer mode and 10ps in fractional mode (with one output divider active and REFCLK jitter excluded). Fractional feedback division accuracy of 27bits is supported.

Modes of Operation

The **Cadence Low-jitter Fractional-N Phase-Locked Loop IP** can operate in three modes: normal, power-down, and bypass.

In the normal mode, the **Cadence Low-jitter Fractional-N Phase-Locked Loop IP** can work as both an integer PLL and fractional PLL. In the power-down mode, the device is powered down and consumes less than 10µA from the core supply and 1µA from the I/O supply. In bypass mode, the reference clock is routed directly to CLKOUTx.

**Cadence IP Factory**

**Cadence IP Factory** can deliver various configurations of Analog IP to meet your design requirements.

With 10+ years of experience and 400+ successful designs in process nodes ranging from 180nm to 22nm, Cadence IP Factory solutions have been proven in everything from low-power MP3 players to leading edge supercomputers.

For more information, visit [ip.cadence.com](http://ip.cadence.com)

Available Products

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Process</th>
<th>VCO frequency (MHz)</th>
<th>I/O supply voltage (V)</th>
<th>Core supply voltage (V)</th>
<th>Input clock frequency (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>IP9200C</td>
<td>UMC 40LP</td>
<td>1000 – 2000</td>
<td>2.25 – 2.75</td>
<td>1.05 – 1.15</td>
<td>19.2 – 40</td>
</tr>
</tbody>
</table>

**Benefits**

- Wide operating range—wide range of input and output frequencies
- Low-power—power down and bypass modes supported
- Compact footprint and low die area

**Deliverables**

- FE views—Layout exchange format (LEF), .lib file, Verilog
- GDSII, netlist (SPICE format for **Cadence Assura® Layout vs. Schematic Verifier (LVS)**)
- Footprint (LEF)
- User documentation, integration guidelines, engineering datasheet
- Silicon validation report (where available)