Overview

Cadence® IP Factory delivers custom, synthesizable IP to support specific design requirements.

The Cadence Multi-Protocol LPDDR4/3/DDR4/3 Controller and PHY Subsystem IP is a combined solution consisting of Cadence Memory Controller IP and Cadence HS DDR PHY IP.

The Cadence Memory Controller IP is extremely configurable to meet the requirements of designs targeting mobile, consumer-enterprise application. Designed with customer-specific configuration in mind, the Cadence Memory Controller IP is an area-optimized solution that includes only required features.

The Cadence HS DDR PHY IP is an all-digital PHY IP consisting of a memory controller interface, external register interface (configuration and test), PHY control block (initialization and calibration logic), and any number of 8-bit data slices. The Cadence HS DDR PHY IP supports operation at twice the frequency of the memory controller and supports key high-speed DDR SDRAM standards, LPDDR4, LPDDR3, DDR4, DDR3, and DDR3L, at speeds up to DDR3200.

The Cadence HS DDR PHY IP is architected to quickly and easily integrate into any system on chip (SoC), and to connect seamlessly to a Cadence, or third-party, DFI-compliant memory controller. The architecture applies innovative features like 4x clocking, multi PLL, and low jitter LC PLL to increase the timing margin available for the system designers to successfully implement high speed DDR systems. Implemented on the TSMC 16FF+ process, the Cadence HS DDR PHY IP provides a cost-effective, low-power solution for demanding applications.

Cadence DDR PHY IP is silicon-proven, with a 10-year history of reliable design-ins, and has been extensively validated with multiple hardware platforms.

Cadence IP Factory offers a comprehensive IP solution that is in volume production, and has been successfully implemented in more than 400 applications.

Key Features

- Support for LPDDR4, LPDDR3, DDR4, DDR3, and DDR3L, at speeds up to DDR3200
- Memory controller: BIST statemachine, RAS features: ECC, RMW, CRC and parity
- Memory controller: port configuration options supporting AMBA® port interfaces
- Memory controller: configurable command queue depth, port bus width and clock interface, arbitration options
- PHY: Register Interface for PHY programming, configuration, and testing modes
- PHY: programmable clock delay (PVT compensated) on read and write datapaths for DQS alignment
- PHY: Memory Controller Interface complies with DFI 4.0, 3.1, 3.0, 2.1, and 2.0
- PHY: LPDDR4/LPDDR3/DDR4/DDR3 training including write-leveling and data-eye training through PHY-independent mode
Product Details

The Cadence Multi-Protocol LPDDR4/3/DDR4/3 Controller and PHY Subsystem IP contains the Cadence HS DDR PHY IP, a classic DQS-delay architecture that uses programmable clock delay lines to align write data, read data capture, and DQS gating from the I/O pads across the DFI interface to the memory controller.

Another part of the subsystem is the Cadence Memory Controller IP, a low-latency, high data rate design that has been tuned to support the highest-speed SDRAMs as well as legacy devices.

Memory Controller

The Cadence Memory Controller IP uses multi-stage reordering algorithms that are capable of delivering 30% performance improvement over the competition (depending on traffic). Performance-tuning parameters, driven from memory model files, allow performance optimization according to individual system and memory requirements.

PHY Architecture

For total control over the DDR interface implementation, the Cadence HS DDR PHY IP provides complete flexibility with process, library, floorplan, I/O pitch, packaging, metal stack up, routing, and other physical parameters.

The Cadence HS DDR PHY IP is implemented with a slice-based architecture, which supports a wide range of memory classes and data rates. The data slice and CA slice provide flexibility for different protocols and data bus widths.

Data Slice and CA Slice

The data slice is an 8-bit wide design that interfaces to the DQ, DM, and DQS connections of the DRAM. The data slice and CA slice provide flexibility to adjust the number of control, command, and address signals as needed.

Benefits

- Low-power control—clock gating
- Low-latency DDR subsystem, DFT support provided
- Feature-rich and application area optimized controller
- Expanded functional testing—datapath loopback

Related Products

- LPDDR4/3 Controller IP
- DDR4/3 Controller IP
- HS DDR PHY IP, TSMC 16FF+
- HS DDR PHY IP is available on several popular processes, and process-specific porting is also available.

Deliverables

- GDS II macros with abstract in LEF for the PHY
- Verilog post layout netlist for the PHY
- STA scripts for use at chip or standalone PHY and controller levels
- Liberty Timing model for the PHY
- SDF for back-annotated timing verification for the PHY
- Verilog models of I/O pads, and RTL for all PHY modules
- Verilog testbench with controller, PHY, memory model, configuration files, and sample tests
- Documentation—integration and user guide, release notes

Available Products

- Multi-Protocol LPDDR4/3/DDR4/3 Controller and PHY Subsystem IP

Figure 2: IP-Level Block Diagram

Cadence Design Systems enables global electronic design innovation and plays an essential role in the creation of today’s electronics. Customers use Cadence software, hardware, IP, and expertise to design and verify today’s mobile, cloud, and connectivity applications. www.cadence.com