Analog Datasheet

802.11n/ac/ad Tri-Band Analog Front End (AFE) IP

TSMC 28HPC

Overview

Cadence® IP Factory delivers custom, synthesizable IP to support specific design requirements.

The **Cadence 802.11n/ac/ad Tri-Band AFE IP** is designed for wireless applications and is capable of supporting high-speed WiFi (802.11n™, ac, and ad) and similar applications.

The **Cadence 802.11n/ac/ad Tri-Band AFE IP** incorporates a dual 7-bit ADC, a dual 7-bit DAC, a PLL, an oscillator, 1:8 data de-multiplexer, 8:1 data multiplexer, and control circuitry.

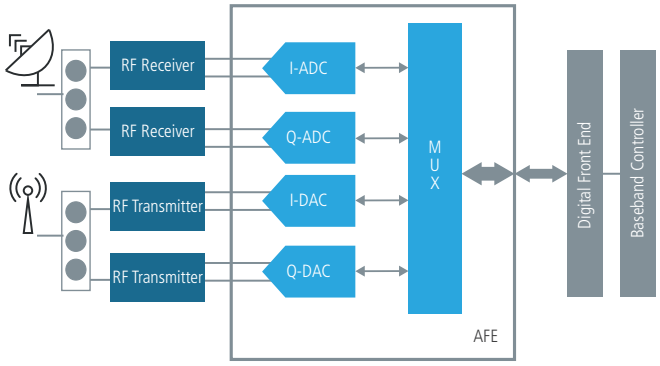

Figure 1: Example System-level Block Diagram

Implemented on the TSMC 28HPC process, the **Cadence 802.11n/ac/ad Tri-Band AFE IP** provides a cost-effective, power-efficient solution for demanding applications. It offers system-on-chip (SoC) implementers the advanced capabilities and support that not only meet, but exceed the requirements of high-performance designs.

The **Cadence 802.11n/ac/ad Tri-Band AFE IP** is based on silicon-proven Cadence ADC and DAC technology.

Cadence IP Factory offers comprehensive IP solutions that are in volume production, and have been successfully implemented in more than 400 applications.

Key Features

- Dual 7-Bit, 3.52GSps ADC
- Dual 7-Bit, 3.52GHz DAC
- Low-jitter 3.52GHz LC VCO Integer or Fractional-N PLL
- Low-power operation and small die area
- Wide operating temperature range: -20°C to 125°C
- Designed for an eight metal layer stackup
- Analog test bus for preproduction testing
- Fast wakeup from the power-down mode

Product Details

The **Cadence 802.11n/ac/ad Tri-Band AFE IP** is characterized by low-power operation and small die area, which makes it suitable for wireless WiGig® applications.

ADC and DAC Blocks

The **Cadence 802.11n/ac/ad Tri-Band AFE IP** incorporates a dual 7- bit ADC and a dual 7-bit DAC that can support sample rates up to 3.52GSps. The dual ADC and dual DAC are both internally synchronized for optimum performance for use in I and Q modulation communication systems.

Crystal Oscillator Circuit

The **Cadence 802.11n/ac/ad Tri-Band AFE IP** contains a low-jitter 54MHz output crystal oscillator circuit, which can operate in either a fundamental or a 3rd overtone configuration.

PLL Block

The **Cadence 802.11n/ac/ad Tri-Band AFE IP** contains a 3.52GHz PLL, which can operate in either an Integer- or a Fractional-N mode. The PLL utilizes an LC VCO architecture to enable high-performance, low-jitter AFE operation. With the PLL and OSC circuit being designed for fast wake up time, the system can go into sleep mode to save power and wake up to check for activities.

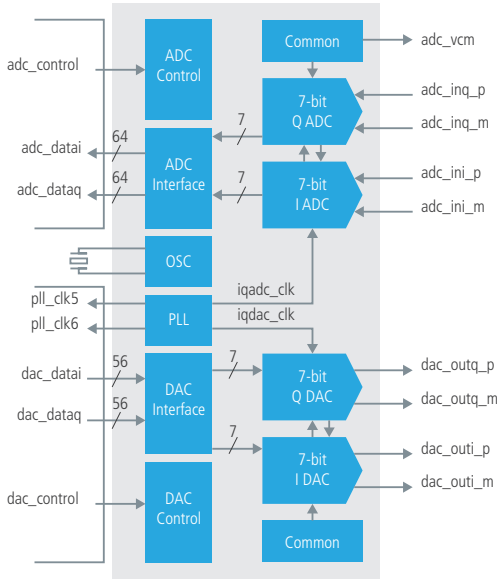

Figure 2: IP-level Block Diagram

Cadence IP Factory

Cadence IP Factory can deliver various configurations of AFE IP to meet your design requirements.

With 10+ years of experience and 400+ successful designs in process nodes ranging from 180nm to 16nm, Cadence IP has been proven in everything from low-power MP3 players to leading edge supercomputers.

For more information, visit ip.cadence.com

Available Products

Part Number	Process	Analog Supply Voltage (V)†	Digital Supply Voltage(V)	Junction Temperature (°C)	RMS Jitter (ps)
IP9937	TSMC 28HPC	0.85 – 0.99, 1.62 – 1.98	0.81 – 0.99	-20 – 125	0.5 (typ.)

† – AVDD, AVDD_H

Benefits

- Fully-integrated solution with clock distribution
- Power-efficient—low power and small die-area
- Architecture-efficient—includes ESD Cells and wiring to bumps
- Low-risk solution— based upon long history of Cadence high-performance, proven data converter technology

Deliverables

- FE views— .lib file, Verilog
- GDSII, netlist (Cadence Physical Verification System for LVS and DRC)
- Footprint (LEF)
- User documentation, integration guidelines, engineering datasheet
- Silicon validation report (where available)
- Integration support

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The IP described in this document may only be taped out and manufactured at a TSMC approved manufacturing facility. Any IC developed from this IP Core must include layer 63 and any other tagging layers (including all tracking tags) as required by TSMC.

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