Overview

**Cadence® IP Factory** delivers custom, synthesizable IP to support specific design requirements.

The **Cadence Dual 11-bit, 1.5GSps ADC IP** is a dual 11-bit ADC with differential inputs. Each ADC supports sustained conversion rates of 1.5GSps.

The **Cadence Dual 11-bit, 1.5GSps ADC IP** supports both single-ended CMOS and differential Current-Mode Logic (CML) clock inputs for maximum flexibility. It also has an 8:1 data multiplexer to reduce data bandwidth from the high conversion rate used by the ADCs to a rate usable by the system logic.

The **Cadence Dual 11-bit, 1.5GSps ADC IP** has clean, well-defined interfaces for easy incorporation into any analog front-end (AFE) or system-on-chip (SoC) design. A Cadence-standard Analog Test Bus is included to facilitate preproduction testing.

Implemented on the TSMC 28HPC process, the **Cadence Dual 11-bit, 1.5GSps ADC IP** provides a cost-effective, power-efficient solution for demanding applications. It offers AFE implementers the advanced capabilities and support that not only meet, but exceed the requirements of high-performance designs.

The **Cadence Dual 11-bit, 1.5GSps ADC IP** is silicon-proven, and has been extensively validated.

**Cadence IP Factory** offers a comprehensive IP solution that is in volume production, and has been successfully implemented in many applications.

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**Key Features**

- Dual 11-bit, 1.5GSps Analog-to-Digital Converters
- Small footprint
- Low power (typ. 475mW at 1.5GHz)
- Multi-level power-down mode
- Internal Reference Generator
- Dynamic power-saving features
- Analog test bus for preproduction testing
- 8:1 data multiplexer
Product Details

The Cadence Dual 11-bit, 1.5GSps ADC IP is a hard macro for the TSMC 28HPC process. Integrated low-capacitance I/O pads are available as an option.

The Cadence Dual 11-bit, 1.5GSps ADC IP supports conversion rates up to 1.5GSps. It is designed to easily integrate into any AFE or SoC design with clean, well-defined interfaces, and separate analog (1.8V and 0.9V) and digital (0.9V) domains.

Master Sample-and-Hold Block

Each ADC in the Cadence Dual 11-bit, 1.5GSps ADC IP contains a Master Sample-and-Hold (S/H) Block with high-impedance differential inputs. The differential inputs help reduce coupled noise and improve conversion accuracy.

SAR Slices

Each ADC also contains eight parallel successive approximation register (SAR) slices. Each SAR Slice converts the output of the Master S/H Block to a 11-bit word, which is passed to the ADC Control and Offset Correction Block for processing.

ADC Control and Offset Correction Block

The ADC Control and Offset Correction Block manages the internal Reference and Timing Generators as well as the individual ADCs. It also has an Offset Correction feature that can remove some offset errors. The Offset Correction feature can be bypassed for sensitive measurement and debugging purposes.

Reference and Timing Generators

The Cadence Dual 11-bit, 1.5GSps ADC IP includes a bandgap reference and all required biasing amplifiers. The bias circuitry can be varied from its nominal set point by a digital control bus to optimize power consumption. All internal reference voltages and bias currents are derived from the bandgap reference.

Figure 2: Single ADC IP Level Block Diagram

Benefits

• High conversion rate to digitize wide-bandwidth signals
• Small footprint
• Low-power—power can be dynamically reduced
• Straightforward integration
• Self-contained reference generator—no external components needed
• High-impedance input buffer
• 8:1 data multiplexer—reduces system clock rate requirements

Deliverables

• Standard integration views—timing, physical views, LEF, DRC, LVS, ANT
• GDSII layout
• Complete documentation customized to your specific configuration

Available Products

• Dual 11-bit, 1.5GSps ADC IP, TSMC 28HPC

Cadence Design Systems enables global electronic design innovation and plays an essential role in the creation of today’s electronics. Customers use Cadence software, hardware, IP, and expertise to design and verify today’s mobile, cloud, and connectivity applications. www.cadence.com

The IP described in this document may only be taped out and manufactured at a TSMC approved manufacturing facility. Any IC developed from this IP Core must include layer 63 and any other tagging layers (including all tracking tags) as required by TSMC.

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