Overview

**Cadence** IP Factory delivers custom, synthesizable IP to support specific design requirements.

The **Cadence 10Gbps EPON/GPON OLT PMA IP** is compliant with the IEEE 802.3av and IEEE 802.3ah standards.

The **Cadence 10Gbps EPON/GPON OLT PMA IP** is a hard macro consisting of a Physical Media Attachment (PMA).

The **Cadence 10Gbps EPON/GPON OLT PMA IP** is designed for Ethernet passive optical network (EPON), gigabit passive optical network (GPON), 1Gb Ethernet (1GE), 10Gb Ethernet (10GE), and SGMII/XFI.

The **Cadence 10Gbps EPON/GPON OLT PMA IP** is architected to quickly and easily integrate into a wide range of network system-on-chip (SoC) applications, including fiber-to-the-home (FTTH), fiber-to-the-building (FTTB), fiber-to-the-curb (FTTC), fiber-to-the-user (FTTU), and gigabit Ethernet.

Implemented on the TSMC 28HPM process, the **Cadence 10Gbps EPON/GPON OLT PMA IP** provides a cost-effective and low-power solution for demanding applications. It offers SoC integrators the advanced capabilities and support that not only meet, but exceed the requirements of high-performance designs.

**Cadence SerDes IP** is silicon-proven and has been extensively validated with multiple hardware platforms.

**Cadence IP Factory** offers a comprehensive IP solution that is in volume production, and has been successfully implemented in more than 400 applications.

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**Key Features**

- Burst-mode clock and data recovery with up to ±200ppm
- Supports mixed data rate and individual lane reset and uses two PLLs at each dual-lane configuration
- Supports serial and parallel loopbacks in symmetrical mode
- Mixed lane pair contexts: GPON/GE, GPON/10GE, EPON/GE, EPON/10GE
- BIST generator and checker for continuous pattern
- Programmable, continuous-time, linear equalizer with 25 levels of adjustments
- Scan chain and analog test bus: debug with built in ADC for analog test measurements

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![Example System-Level Block Diagram](image-url)
Product Details

The Cadence 10Gbps EPON/GPON OLT PMA IP is a hard PMA macro for the TSMC 28HPM process. Integrated I/O pads and ESD structures are available as an option.

PHY Architecture

The Cadence 10Gbps EPON/GPON OLT PMA IP is designed with a slice-based architecture, providing greater control over floorplanning, placement, packaging, and I/O integration than other hard PHY solutions while maintaining reliability and ease of use associated with GDSII macros.

Extensive testability offers users the on-chip oscilloscope, multi loop-back options, PHY stand-alone functionality with SoC isolation and at-speed scan support.

Cadence IP Factory

Cadence IP Factory can deliver various configurations of SerDes IP to meet your design requirements.

With 10+ years of experience and 400+ successful designs in process nodes ranging from 180nm to 16nm, Cadence IP has been proven in everything from low-power MP3 players to leading edge supercomputers. As an active member of many standards organizations, Cadence has early insight into emerging standards, and can quickly and easily adapt to critical and important changes to current standards.

For more information, visit ip.cadence.com

Benefits

- Low-risk solution—hardened and silicon-proven design
- Ease of integration—system integration kit reduces system integration and signal integrity issues
- Mixed-rates flexibility—dual-lane with dual PLL design enables the use for different data rates between lanes

Related Products

- Controller IP for PCIe 1.0/2.0
- Controller IP for PCIe 3.0
- 10G-KR Multi-Protocol PHY IP
- Ethernet Triple PHY IP

Deliverables

- Standards integration views: timing, Verilog behavior, physical views, LEF, DRC, LVS, ANT
- GDSII layout
- Documentation — integration and user guide, release notes
- Sample verification testbench

Available Products

- 10Gbps EPON/GPON OLT PMA IP, TSMC 28HPM

![Figure 2: IP-Level Block Diagram](image-url)