

Simulation VIP for SRIO 3.0

Overview

Cadence® Simulation VIP is the world’s most widely used VIP for digital simulation. Hundreds of customers have used Cadence VIP to verify thousands of designs, from IP blocks to full systems on chip (SoCs).

The Simulation VIP is ready-made for your environment, providing consistent results whether you are using Cadence Incisive®, Synopsys VCS®, or Mentor Questa® simulators. You have the freedom to build your testbench using any of these verification languages: SystemVerilog, e, Verilog, VHDL, or C/C++. Cadence Simulation VIP supports the Universal Verification Methodology (UVM) as well as legacy methodologies.

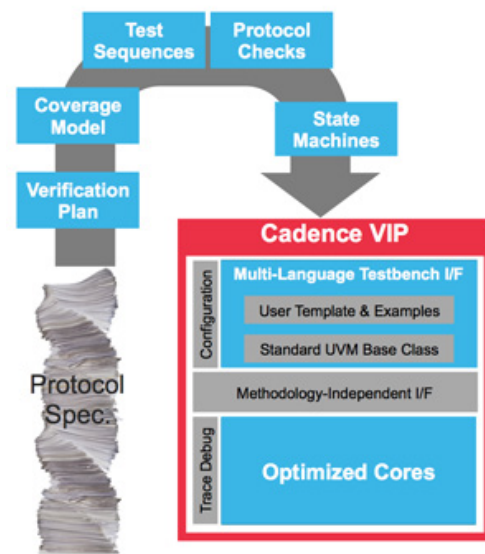
The unique flexible architecture of Cadence VIP makes this possible. It includes a multi-language testbench interface with full access to the source code to make it easy to integrate VIP with your testbench. Optimized cores for simulation and simulation-acceleration allow you to choose the verification approach that best meets your objectives.

Specification Support

The SRIO 3.0 VIP supports SRIO Protocol versions 3.0 as defined in the SRIO Protocol Specification.

Supported Design-Under-Test Configurations

- | | | |
|--|--|-------------------------------------|
| <input checked="" type="checkbox"/> Host | <input checked="" type="checkbox"/> Device | <input type="checkbox"/> Hub/Switch |
| <input checked="" type="checkbox"/> Full Stack | <input type="checkbox"/> Controller-only | <input type="checkbox"/> PHY-only |



Deliverables

People sometimes think of VIP as just a bus functional model (BFM) that responds to interface traffic. But SoC verification requires much more than just a BFM. Cadence Simulation VIP components deliver:

- State machine models incorporate the subtle features of state machine behavior, such as support for multi-tiered, power-saving modes
- Pre-programmed assertions that are built into the VIP to continuously watch simulation traffic to check for protocol violations.
- Test suites are provided for most Cadence VIP components.
- Pre-programmed coverage models used to capture interesting combinations of simulation results. By analyzing the results collected by the coverage model, engineers can tell if the simulations have exercised the various modes of operation of an interface.
- Verification plans for most protocols link the “raw” coverage model results back to the protocol specification.

Key Features

- | | |
|--|--|
| • Input/Output packet formats are supported | • Message passing architecture and packet formats are supported |
| • Globally shared distributed memory model architecture and packet formats are supported | • Flow Control Logical Layer management based on source, destination and physical channel is supported |
| • Data Streaming Logical specification is supported | • Currently, only 1x is supported |
| • Both IDLE1 and IDLE2 sequences and therefore Short and Long Control Symbols are supported | • Multiple virtual channels on PHY are supported |
| • Both reliable and continuous traffic (RT and CT) are supported | • Both receiver-ended and transmitter-controlled flow control on Physical Layer are supported |
| • EndPoint Device features are supported | • Both small and large device IDs are supported |
| • Support for 64b/67b encoding: codewords, ordered sequences, and IDLE3 | • Support for 10.3125 Gbaud lane speed |
| • Increase ackID size for IDLE3 to 12 bits | • Support for large packets, Dev32 |
| • Specific link initialization state machines to support initialization of 10.3125 Gbaud links | • Asymmetric operation of 10.3125 Gbaud links |
| • Allowed Packet Accepted control symbols to acknowledge multiple packets | • Input/output error recovery protocol updated in order to enable faster recovery |
| • New per-port register block format, with new/modified registers | • Added time synchronization support |

Test Suite

This VIP includes a basic test suite capability that includes:

- Constrained-random example tests
- 3rd party simulator test execution



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