VIP Datasheet

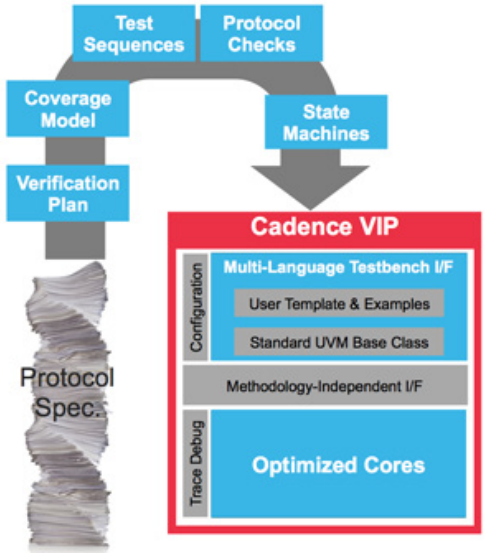
Simulation VIP for Mobile High-Definition Link (MHL)

Overview

Cadence® Simulation VIP is the world's most widely used VIP for digital simulation. Hundreds of customers have used Cadence VIP to verify thousands of designs, from IP blocks to full systems on chip (SoCs).

The Simulation VIP is ready-made for your environment, providing consistent results whether you are using Cadence Incisive®, Synopsys VCS®, or Mentor Questa® simulators. You have the freedom to build your testbench using any of these verification languages: SystemVerilog, e, Verilog, VHDL, or C/C++. Cadence Simulation VIP supports the Universal Verification Methodology (UVM) as well as legacy methodologies.

The unique flexible architecture of Cadence VIP makes this possible. It includes a multi-language testbench interface with full access to the source code to make it easy to integrate VIP with your testbench. Optimized cores for simulation and simulation-acceleration allow you to choose the verification approach that best meets your objectives.



Specification Support

Cadence MHL VIP is compliant with MHL specification version 3.0. The specification is developed by the MHL Consortiumhttp://www.mhlconsortium.org/ and is available only for licensed users.

Supported Design-Under-Test Configurations

☑	Master	☑	Slave	☐	
☑	Full Stack	☐	Controller-only	☐	PHY-only

Deliverables

People sometimes think of VIP as just a bus functional model (BFM) that responds to interface traffic. But SoC verification requires much more than just a BFM. Cadence Simulation VIP components deliver:

- State machine models incorporate the subtle features of state machine behavior, such as support for multi-tiered, power-saving modes
- Pre-programmed assertions that are built into the VIP to continuously watch simulation traffic to check for protocol violations.
- Test suites are provided for most Cadence VIP components.
- Pre-programmed coverage models used to capture interesting combinations of simulation results. By analyzing the results collected by the coverage model, engineers can tell if the simulations have exercised the various modes of operation of an interface.
- Verification plans for most protocols link the "raw" coverage model results back to the protocol specification.

Key Features

- Supports RGB, YCbCr 4:4:4 and YCbCr 4:2:2 MHL specification
- Supports both 24bits and 16bits per pixel mode
- Supports various 3D video frame formats
- Supports custom frame formats that allow users to configure frame formats that are DUT specific and not defined in the specification
- Supports all packet types defined in the MHL 3.0 Specification
- Supports serial and symbol interface types
- Supports verification of both Source (Tx) and Sink (Rx) device types
- Supports user configurable, vendor specific Info-Frame Packets
- MSC commands supported - SET_HPD, CLEAR_HPD, READ_DEV_CAP, WRITE_STAT, SET_INT
- DDC commands supported - DDC_READ, DDC_WRITE
- Supports Wake Pulse Sequence and Discovery Pulse Sequence
- Supports MHL 2.0 - Both PixelPacking mode and normal mode

Test Suite

This VIP includes a basic test suite capability that includes:

- Constrained-random example tests
- 3rd party simulator test execution

Related Products

- HDMI 1.4 Simulation VIP
- HDMI 2.0 Simulation VIP

cadence

Cadence Design Systems enables global electronic design innovation and plays an essential role in the creation of today's electronics. Customers use Cadence software, hardware, IP, and expertise to design and verify today's mobile, cloud, and connectivity applications. **www.cadence.com**