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Verification of SSIC Design Using Cadence SSIC VIP

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Introduction

SuperSpeed Inter-Chip (SSIC) is a "chip-to-chip" interconnect that allows users to combine USB 3.0 designs over MIPI Mobile PHY (M-PHY) to provide a high-speed and low-power interface for on-board inter-connectivity.

For example, SSIC can be used to connect a mobile applications processor to a 3G/4G baseband chip as shown in Figure 1. The applications processor could use the same, unmodified USB drivers it uses for an external USB plug-in 3G/4G modem. It uses USB 3.0 to communicate, but uses less power because of the low pin signal interface. It does not use a standard USB 3.0 cable but, instead, a different M-PHY interface for SSIC. The M-PHY interface can be shared between the low latency interface (LLI) and SSIC. Figure 1 shows a device under test, featuring a SSIC device with M-PHY.

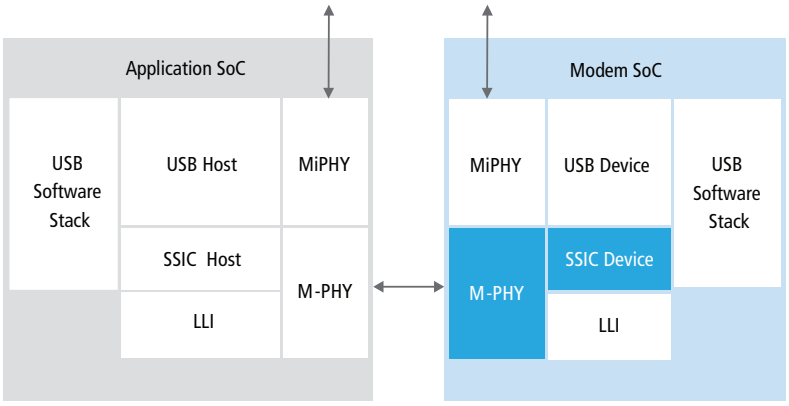

Figure 1. Example Usage of Subsystem

SSIC Functional Overview

SSIC defines a chip-to-chip USB-based interconnect for mobile devices as well as other platforms. SSIC offers the MIPI Alliance's M-PHY high-bandwidth and low-power capabilities combined with SuperSpeed USB performance enhancements.

The M-PHY interface, a high-speed serial interface, targets up to 2.9Gbps per lane with scalability up to 5.8Gbps per lane, and offers a low pin count and exceptional power efficiency. SuperSpeed USB offers a 5Gbps signaling rate, up to 10X faster than Hi-Speed USB (USB 2.0), as well as an enhanced protocol and power management and software model.

Demand for higher speeds in mobile consumer applications, such as video streaming, calls for a more efficient interface, and SSIC fits right there.

The USB-IF aligned SSIC with the MIPI Alliance's M-PHY, a gigabit-speed, on-PCB, chip-to-chip PHY. The M-PHY standard consumes lower power and offers greater flexibility than USB 3.0 PHYs. M-PHYs can come in three speeds, called Gears. Gear1 operates at 1.25 or 1.45Gbps, Gear2 at 2.5 to 2.9Gbps, and Gear3 up to 5.8Gbps. In addition, M-PHYs can have one, two, or four lanes. Each lane has x pins, so two lanes have 2x pins and four lanes have 4x pins. These lane configurations offer flexibility to run either in multiple parallel lanes at slower clock speeds to save power, or to run at faster speeds but consume fewer pins.

The interface has the following key attributes:

- Support for the SuperSpeed (USB 3.0) protocol
- Up to 5Gbps maximum data rate supported
- Optimized for low power, area, cost and EMI robustness for embedded inter-chip links
- Compliant with Type-I M-PORTs from the MIPI M-PHY

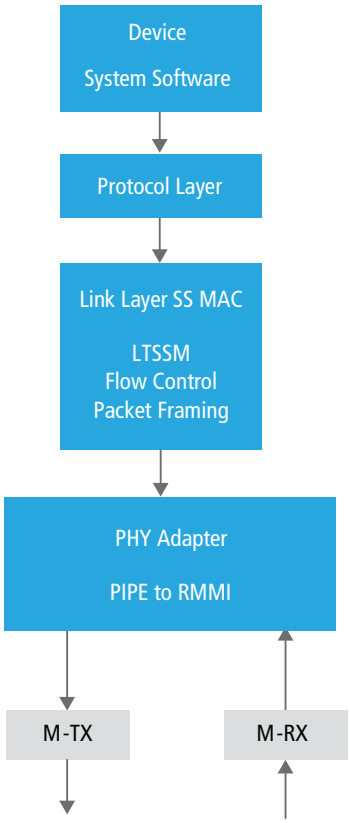

Figure 2. Full Stack Diagram of the SSIC Subsystem

SSIC - What's different from USB 3.0

- No backward compatibility with USB 2.0 or High-Speed Inter-Chip (HSIC)
- No receiver detection or LFPS signaling for SSIC
- Notable differences in LFSR (scrambling) rule:
  - MK0 (COM) of HS-BURST will reset LFSR
- Different LTSSM states and transitions mapped to M-PHY states:
  - SLEEP
  - STALL
  - HIBERN8
  - HS-BURST

  - PWM-BURST
  - LINE-RESET
  - DISABLED
- Line states - DIF-P(1/0), DIF-Z(Z/Z), DIF-N(0/1)

SSIC - LS-Mode (RRAP)

- Remote Register Access Protocol (RRAP)
  - Separate register space (rrap) address map
- Incorporates a “low-speed ” RxDetect.LS-MODE LTSSM state
- Happens during PWM burst mode
  - PWM-G1 burst (3Mbps - 9Mbps)
- Communications happens via read/write command and responses through PAIR0 (Lane 0)
- Downstream port is a master and upstream port is a slave
- M-PHY capability, configuration, and status attributes and PAIR capability attributes are configured through RRAP communication
- Test mode

SSIC - LS-Mode (PWM-Burst)

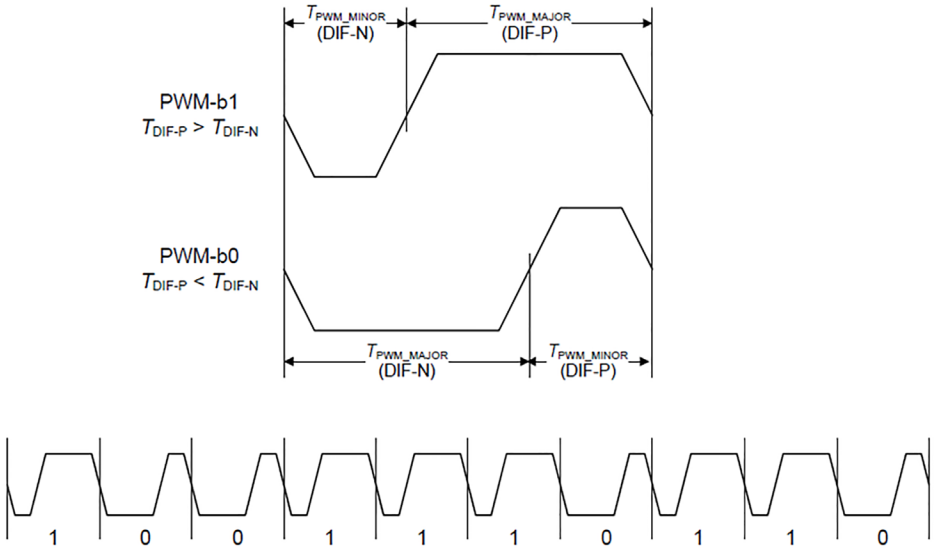

Figure 3. PWM Bit Waveforms and Bit Stream Example (Source: M-PHY Specification)

Each bit consists of a combination of two sub-phases, a DIF-N followed by a DIF-P. One of the two sub-phases is longer than the other: *TPWM_MAJOR > TPWM_MINOR, depending upon whether a binary one or binary zero is being sent.*

SSIC - LTSSM

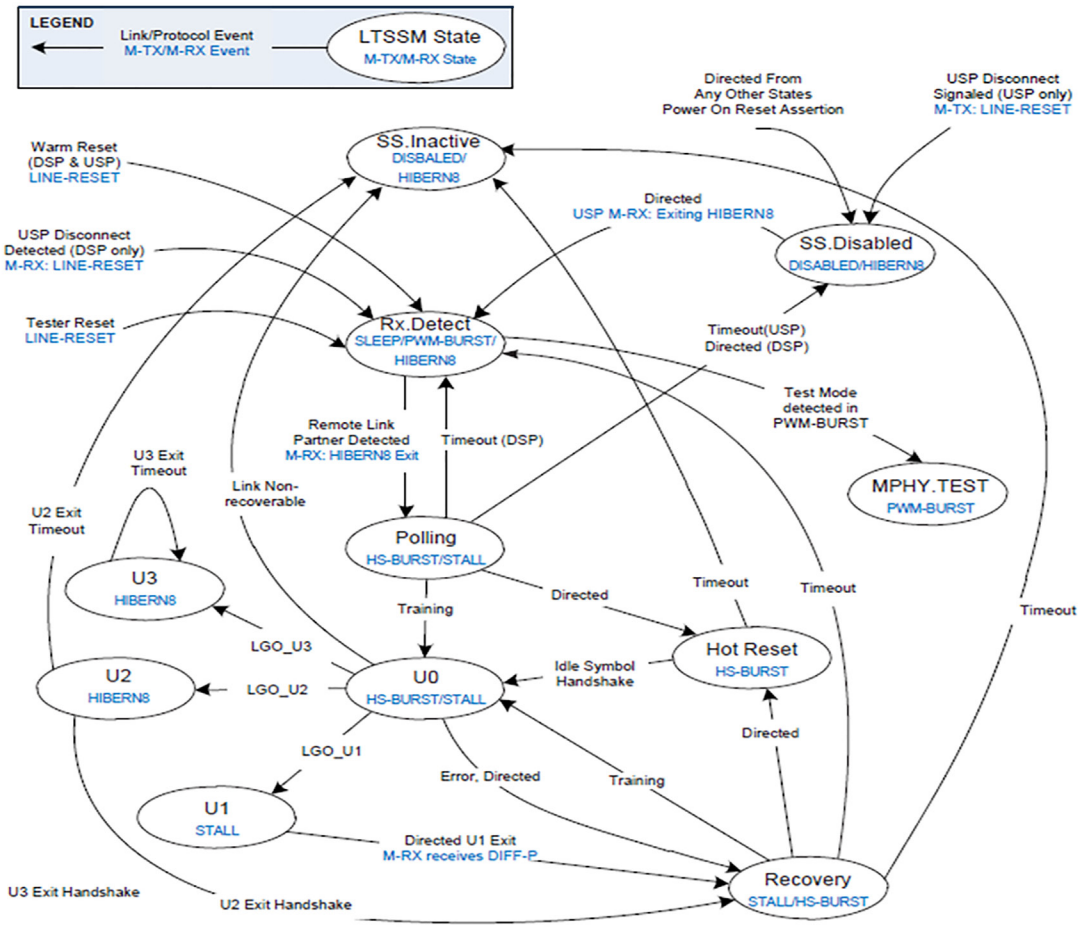

Figure 4. SSIC LTSSM State Diagram (Source: SSIC Specification)

- M-PHY states are mapped to LTSSM states
- Polling.STALL LTSSM state instead of Polling.LFPS state
- SS data is transmitted in HS-BURST states
  - Polling, recovery, U0, hot reset
- HS-BURST
  - PREPARE
  - SYNC
  - Payload (always starts with MK0, a.k.a. COM symbol)
  - Tail of burst
- PWM-Burst
  - PREPARE
  - Payload (always starts with MK0, a.k.a. COM symbol)
  - Tail of burst

SSIC Design Challenges

Before looking at the design challenges, it would be worthwhile to discuss how the SSIC subsystem is implemented so that specific design challenges can be understood. The figure below gives the conceptual block diagram of the SSIC subsystem.

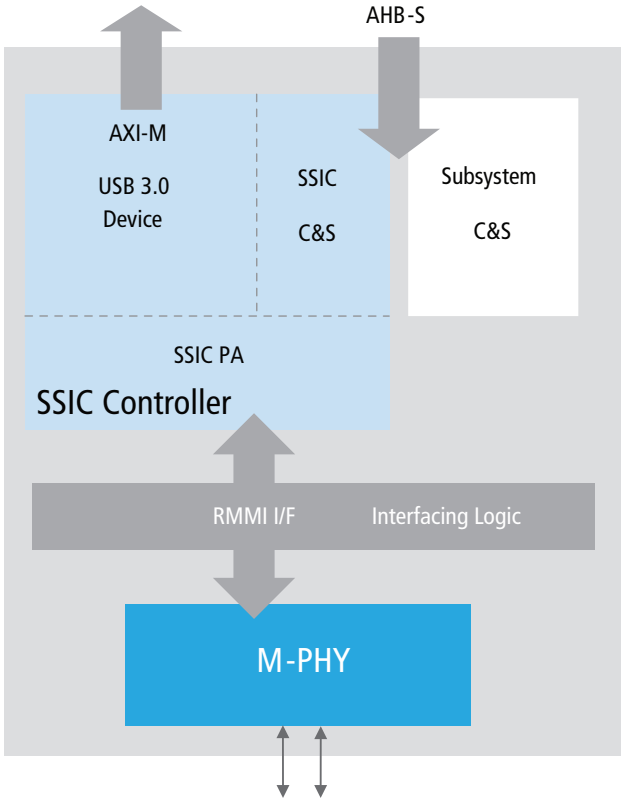

Figure 5. SSIC SS Architecture

Two major components of the subsystem are the "SSIC controller" and the "MIPI M-PHY," and they are procured from different and independent sources. The subsystem also has a general subsystem C&S (control and status) block which lets the system CPU control and monitor various aspects of the subsystem. The SSIC controller and M-PHY are connected through an interfacing logic that connects the two and also implements other subsystem requirements.

Below, and classified based on functional requirements, are various design challenges faced during the implementation of the subsystem.

SSIC controller—M-PHY RMMI interoperability

As the two components originate from different and unrelated sources, the foremost requirement was to ensure interoperability at the RMMI signaling level. There were issues seen at this level specifically in areas where SSIC specs provide freedom of implementation. Such cases were discussed with the two providers, and corner cases analyzed and verified to ensure interoperability at the RMMI interface.

SSIC controller—M-PHY capability/configuration interoperability

M-PHY is a highly configurable PHY with various operational parameters that can be changed on the fly. SSIC specs set specific limits for M-PHY capabilities, which M-PHY should be supported and with which the controller should interoperate. Additionally, the M-PHY capabilities should also be interoperable with the remote partner (host) capabilities.

These two levels of interoperability were analyzed and M-PHY, though actually implementing the required capabilities, had the wrong representation of the capabilities in its registers. This could have confused the remote host when it read the capabilities during RRAP; hence, an update of the values in these capability registers was needed.

Also, since the SSIC controller is a new implementation, simulations were observed to understand the implementation of the specific SSIC/M-PHY parameters, including their handling and alignment with the specs. For example, one of the parameters, MIN_ACTIVATE_TIME, had more reliable implementation within the M-PHY. The M-PHY's capability to control this timing was used instead of the default controller option.

Overall, due to the configurability of these parameters, the end-to-end (device controller->device M-PHY-> host M-PHY-> host controller, and reverse) parameter interoperability becomes a challenge and needs to be thoroughly verified.

USB3 LTSSM- M-PHY state machine interoperability

USB 3.0 primarily uses LTSSM (Link Training and Status State Machine), whereas M-PHY uses state sequences which are apparently unlinked to USB3 LTSSM. SSIC specs try to link these two different and unlinked state machines to implement a workable low-power inter-chip communication solution.

Since this SSIC subsystem was the first implementation of the SSIC specs with various given components, it was important to ensure that state machines/signaling/transitions are in sync at all the following levels:

1. M-PHY serial interface
2. M-PHY state machine
3. RMMI parallel interface
4. USB 3.0 LTSSM

The behavior at all four levels was observed and corroborated with the SSIC specifications.

SSIC boot-up requirements

The original approach to program the local M-PHY and to respond to host RRAP commands within the controller was based on SSIC interrupts where typically four interrupts are generated per RRAP command. This meant that the SSIC controller moved to operational U0 state after taking a significant amount of time, which was unacceptable.

Later down the project, a full hardware-based solution was introduced in the SSIC controller with the system latencies totally removed. This also required additional logic implementation within the subsystem integration and, hence, the increased verification needs.

However, the SSIC controller provided only the options of fully manual or fully automated "local M-PHY programming/RRAP response". The subsystem implemented functionality to allow software intervention even in fully automated operation, allowing the customization of some of the programming in fully automated mode.

SSIC low-power support in U2 and U3

USB 3.0 uses PowerMode[1:0] signals to manage the power states of the USB 3.0 PHY, whereas for SSIC's RMMI interface, there is no such mechanism for specifying the power state that a USB 3.0 state machine LTSSM might be in to the M-PHY.

There are advanced power savings possible in M-PHY when USB 3.0 is in U2 and U3 and M-PHY should be accordingly managed. But the custom register-based power management approach of the M-PHY is unknown to the USB 3.0 specs and not implemented in the SSIC controller physical adaptation (PA) layer.

This problem required the following to be implemented:

1. M-PHY was updated to provide advanced power control as a few signals at the M-PHY periphery
2. The "Interfacing Logic" took the LTSSM state from the SSIC controller and appropriately managed the M-PHY advanced power management signaling based on the state of the SSIC LTSSM

This turned out to be fairly complex logic with the additional possibility of introducing delays between power events detection and power management signaling to the M-PHY so that power savings could be fully optimized. This led to the very efficient and fully hardware-automated M-PHY power management in U2/U3 and other LTSSM states.

SSIC subsystem hibernation support in U3

The hibernation support means that it is possible to power-down the whole SSIC controller and the majority of the M-PHY lying in VCore when the subsystem is in U3. A small portion within "Interfacing Logic" and M-PHY is in VSafe and remains powered up so that any wakeup events may be detected. The "Interfacing Logic" detects the wakeup and signals the system to power on the VCore.

M-PHY hibernation was supported through an out-of-band signaling approach as needed by M-PHY-related standards. SSIC required a small update in M-PHY to support in-band wakeup where long DIF-N signaling can be used to bring the SSIC subsystem out of hibernation.

There was an anomaly in the SSIC controller regarding hibernation support. It assumed that M-PHY is always powered ON when it itself goes into hibernation. This was, however, not the case. Our hibernation approach envisaged that advanced power savings could be achieved by powering down the M-PHY, especially when this feature was already available within M-PHY. Needed design and programming updates were done in the SSIC controller to support hibernation, with a major portion of the M-PHY powered down.

When all the components were OK to support hibernation in a desired manner, the next challenge was to implement the overall hibernation strategy and RTL infrastructure. This was done in the PMUs within the "Interfacing Logic".

Additional control/status/events

Given the first-time use case for SSIC, it was important to provide a full-pronged implementation to act should any undesired situations within the subsystem occur. This required the following features within the "Subsystem C&S" block:

- Provision of interrupts covering events not covered by SSIC controller and for important events on the RMMI interface
- Possibility to monitor and force important signals on the RMMI interface on the SSIC controller
- Possibility to monitor and force important signals on the RMMI interface on the M-PHY
- Control and status of various signals within the SSIC subsystem

Only a few use cases for these were seen, but they still had to be designed and verified to provide intervention possibilities whenever needed.

SSIC Verification Challenges

SSIC protocol verification provides an added complexity to verify a USB 3.0 fused with M-PHY design.

Development of verification IPs (VIP) for such complex protocols is extremely challenging considering that users are looking to minimize test runtime and memory consumption impact. Also adding to the challenge is the fact that users are looking at using different platforms and languages for doing verification at the block, sub-system, and SoC levels.

To make sure that the design is properly verified, all the supported formats have to be checked with all the possible configuration settings.

Some typical features for SSIC verification include:

- Link training
- All LTSSM transitions
- RRAP transfers capability
- Full RRAP

- SuperSpeed data transfers bulk-in/out
- PWM burst mode
- HS transfers for all gears for Series A and B devices
- Warm reset
- Low-power mode
- Power aware (UPF 1801)
- USP/DSP connect/disconnect
- Loopback test mode

Cadence SSIC Verification IP and Experience

Silicon design houses are constantly looking to reduce the time to market (TTM) for their products. Extremely aggressive timelines and limited resource allocation require them to have highly adaptable test and verification environments for their SoCs. This essentially means plug-n-play verification components, which are generic in design and configurable for different environments, e.g. platforms, languages, capabilities, etc.

The Cadence® SSIC VIP is built on top of the Cadence USB 3.0 VIP, which is already a proven solution used worldwide for USB 3.0 module/SoC verification.

SSIC layer is added as another PHY interface over the existing and proven USB 3.0 VIP. It employs the concepts of Specification of Modeling Architecture (SOMA) callbacks, registers, and queues, and provides significant ease of use in plug-and-play terminology.

To cater to the requirements of a vast majority of silicon design houses, a highly flexible, scalable, and proven VIP development methodology is adopted. The methodology is carefully architected such that the developers have enough flexibility to add desired VIP-specific capabilities, e.g. protocol checkers or data checkers, and at the same time can keep a check on the memory footprint and CPU runtimes.

To be able to thoroughly verify the design under test (DUT), VIP needs to be robust and at the same time provide enough flexibility and configurability to the user so as to cover all the typical as well as corner case scenarios. Some of the features for Cadence SSIC VIP are listed below:

- Available in both serial and RMMI interface over multi-lane support
- Can be configured for all different HS gears for Series A and B devices
- Static configuration parameters as per specifications, which are constant across different set modes and traffic, are configured by default with full flexibility to scale down for higher simulation efficiency and lower simulation times
- Can initiate RRAP commands and responses automatically with support available for user-defined RRAP communications as well
- Provides “backdoor access” to configure SS and RRAP/M-PHY capability attributes
- Baseline architecture remains the same irrespective of HVL or methodology used
- Provides complete support to cover all LTSSM arc transitions, directed or undirected
- Lower power modes, USP/DSP connect/disconnect and test mode

Verification Environment for a Typical SINK DUT

The SSIC subsystem has the upstream mode port (device). The heart of the SSIC subsystem is the third-party controller. It also consists of the glue/wrapper logic, power controller, and memories.

M-PHY is compliant with Type–I and single lane. The subsystem is supposed to operate on PWM-G1 for LS-mode and HS-G1 Rate B for HS-mode of operation. The behavioral model of the M-PHY is used for the simulation.

The SSIC subsystem has an ARM® AMBA® AHB slave interface for configuration and AMBA AXI master interface for data transfer. It has two interrupts: 1) USB interrupt (to handle the legacy USB-specific events such as device or endpoint events) and 2) SSIC interrupt (to handle the SSIC-specific event such as local M-PHY configuration or RRAP event). The SSIC subsystem has a 40-bit RMMI (reference module M-PHY interface) parallel interface to connect with the serial PHY (M-PHY). The RMMI interface can be categorized for M-TX and M-RX, which can be further divided between control and data as shown in the following figure. RMMI RX/TX CFG interface configures the local M-PHY attributes.

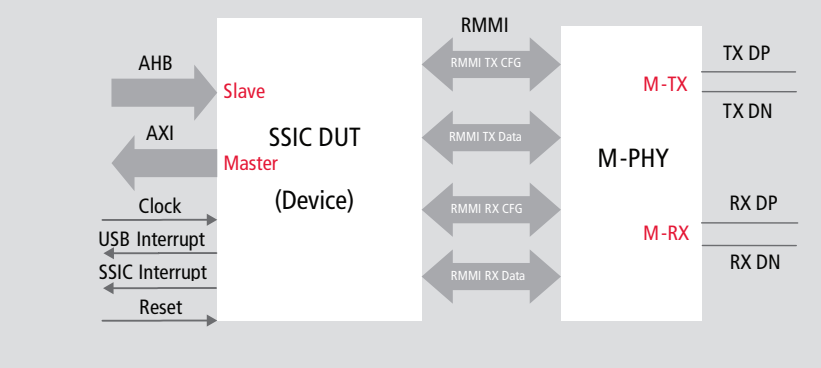

Figure 6. SSIC Subsystem Interfaces

To create the verification environment for SSIC verification, a SystemC/TLM platform has been deployed to imitate the processor-based verification. An SSIC driver developed on top of the USB device driver is used for the configuration. As shown in the following figure, the processor configures the subsystem through the AHB interface.

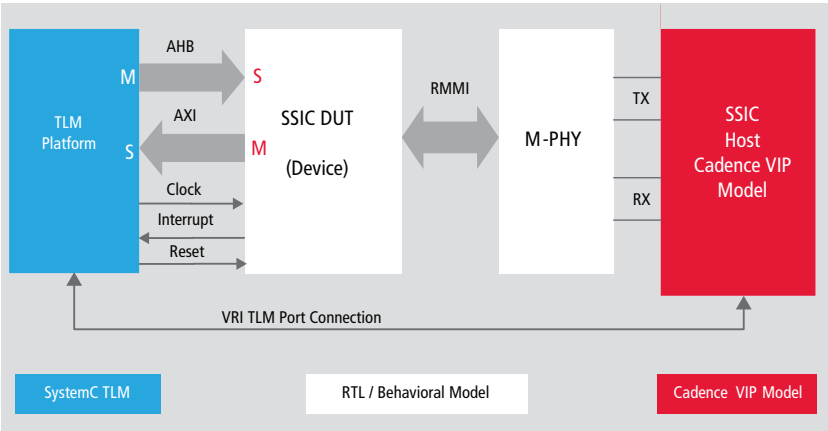

Figure 7. SSIC Subsystem Verification Environment

The active mode of the SSIC VIP host model is used for RTL verification of the SSIC device. The passive mode of the SSIC VIP device model is plugged as the monitor (for simplification purposes, it has been omitted from the above figure), which can be useful for the compliance check. The host model is statically configured through SOMA (Specification of Modeling Architecture) and registers.

The VIP and DUT can be configured to reduce the simulation time. SSIC VIPrc file configuration can be categorized for enumeration as the following:

Bypass Enumeration: The capabilities of the device are read through the SOMA file directly. No control transfer is initiated by the host model. A pre-defined device address is assigned at both ends. The device controller is configurable to bypass the set address phase.

Enumeration: The device capabilities are read by the host through enumeration.

RRAP commands are issued by the host to align the host M-PHY with the device M-PHY. Typically, the number of attributes is very high for any M-PHY, which results in a large number of RRAP commands.

Minimal RRAP: To reduce the simulation time, minimal RRAP commands are performed by the host, and rest of the device M-PHY attributes are read by the SOMA.

Full RRAP: The host performs the RRAP as per the SSIC specification.

Once an SSIC device and SSIC host are entered into the U0 LTSSM state, data can be exchanged in the HS-mode. Virtual register interface (VRI) is used to trigger the host VIP model on-the-fly from the software running on the processor. VRI, a Cadence solution to configure VIP and effectively interface from C embedded tests, is used for the dynamic configuration of the VIP host model. VRI interface is also used for the scoreboard mechanism.

The aim of subsystem verification is to cover the subsystem integration and inter-operability scenario. The verification test scenarios cover various LTSSM transitions. We have ensured the data integrity by performing the bulk transfer. In addition, there were scenarios created to perform control transfer between the device and the host-generated sequence. The RTL verification of SSIC SS was performed with SSIC VIP from Cadence. A few scenarios are described as follows:

RRAP test case (RxDetect -> polling -> U0): RRAP commands are exchanged between host and device in the RxDetect LTSSM state. Successful entry of the device into U0 LTSSM state will ensure the correct RRAP operation.

Bulk transfer test case: In the U0 LTSSM state, the host and device are ready to exchange the data. We prepare the transaction request block (TRB) and the data packets in the system memory. Endpoints are configured for bulk in and bulk out operation. VRI call is used to trigger the bulk operation.

U1/U2/U3 test case: For U1/U2/U3 entry, software running on the processor triggers the host SSIC VIP model by VRI. The U1/U2/U3 exit can be initiated by either host or device. Bulk data is exchanged between host and device in the U0 LTSSM state.

Warm-reset, USP disconnect and DSP disconnect: Disconnect and warm reset are mapped on the line-reset feature of the M-PHY.

The verification environment developed at the subsystem level, which includes the VIP configuration files and software drivers, is easily portable in the SoC verification environment. The SSIC VIP model is designed such that it is reusable both vertically (subsystem to SoC) and horizontally (one project to another project if the configuration is the same).

Conclusion

As a novel technology, there have been some concerns on interpretation of specifications for SSIC among various vendors providing IP components, VIP, etc. Because interoperability of the SSIC subsystem has been a main concern, it is important to perform functional verification to qualify subsystem components together. Cadence VIP was chosen to achieve the objective, followed by an evaluation with an initial ad-hoc setup.

Other conclusions are as follows:

- Interoperability between the USB 3.0 controller and the M-PHY is a main challenge with the SSIC subsystem
- Early availability of SSIC VIP accelerated the ramp up of the SSIC subsystem verification environment
- The subsystem verification environment, including the VRI drivers and the same SSIC VIP configuration, is reusable at the SoC level