VIP Datasheet

# Acclerated VIP for Ethernet 40G/100G

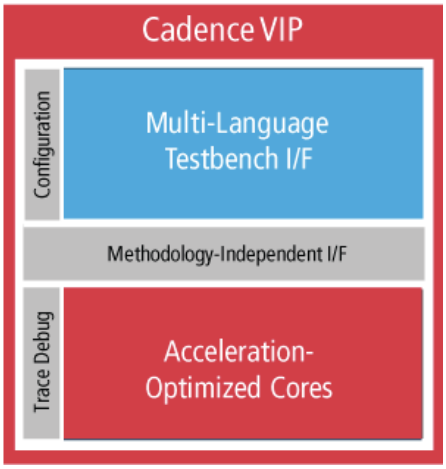
## Overview

Sometimes chips are just too big to verify with logic simulation software. SoCs comprised of tens of millions of logic gates will bog down software simulators, even when running on the fastest servers.

Simulating big designs requires hardware-assisted verification, an approach that uses special-purpose hardware, like Cadence® Palladium® XP systems, to dramatically boost simulation performance.

Cadence Accelerated VIPs are complementary products to Cadence simulation VIP and SpeedBridges. Accelerated VIPs are used to funnel data to the user's design-under-test and respond to stimulus received from it. Monitor functions such as collecting coverage and setting callbacks are not included.

Tuned for performance, AVIPs are an integral component in a simulation acceleration environment, speeding up verification 10's to 1,000's of times relative to simulation. The level of acceleration gain is dependent on the user's individual testbench and DUT synchronizations.




## Specification Support

The Ethernet AVIP is compliant with the IEEE Standard 802.3.

## Usage Options

- [x] Simulation Acceleration
- [ ] HW/SW Co-Verification

## Supported Design-Under-Test Configurations

- [x] MAC
- [x] PHY
- [ ] Hub/Switch
- [x] Full Stack
- [x] Controller-only
- [x] PHY-only

## Product Highlights

**40G and 100G MAC Features**

- XLGMII interface for Ethernet 40G
- CGMII interface for Ethernet 100G
- 64/128/192 bit configurable XLGMII/CGMII to the Physical layer
- Full duplex operation
- Automatic preamble, pad, and CRC generation on transmitted frames
- Jumbo frames of up to 9K bytes
- Pause frames
- 802.1Q VLAN tagging with recognition of incoming VLAN and priority tagged frames
- 802.1Qbb priority-based flow control

**Other Supported Features:**

The Ethernet AVIP supports all types of Ethernet transactions, including:

- Ethernet v2 frames, Ethernet 802.3 frames
- Pause frames
- Priority pause frames
- Jumbo frames
- VLAN tagged frames

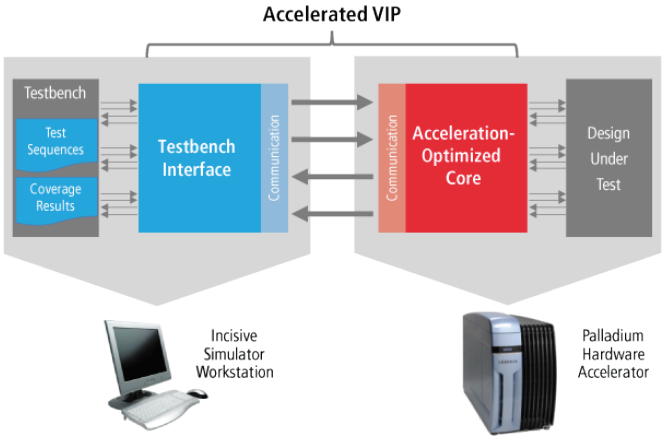
The following upper-layer frame formats are now supported in C++ mode as beta features:

- TCP and UDP frame formats
- IPv4 and IPv6 frame formats
- SNAP and MPLS variants of IPv4 / IPv6 / TCP / UDP
- Double VLAN tagged frames

## Simulation Acceleration

In simulation acceleration, the Cadence Palladium XP system works in conjunction with the Cadence Incisive® Simulator to divide up the simulation task. The Palladium XP runs the design under test while the Incisive simulator runs the testbench. Accelerated VIP is inserted for each of the standard interfaces in the design with the testbench interface running on Incisive and the acceleration-optimized core running on the Palladium XP.

Most of the testbench components employed in simulation can be reused, which saves set-up time and preserves the controllability and observeability of traditional logic simulation. With this approach, performance is often up to 1000X faster than logic simulation.

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