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Five Key Challenges in Designing with High-Speed Analog IP

By Bob Salem and Kevin Yee, Cadence Design Systems

Though we might feel as if we live in a digital-centric world, in the realm of chip design, analog circuitry continues to play a critical role. It is particularly essential with the rise of Internet of Things and mobile applications that interact with the analog "real" world. However, designing with analog intellectual property (IP) to support these high-end designs comes with vastly different challenges when compared to supporting low-end applications. This paper examines five key challenges that design engineers must address to successfully design with analog IP.

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Introduction

Stop for a moment…what do you see?

Close your eyes…what do you hear?

Reach out your hand…what do you feel?

The answers to these questions are all analog. From air conditioning systems with temperature sensors to TVs controlled by touchscreens, our connected world is marked by an abundance of mobile, Internet of Things, and wireless applications that rely on mixed-signal systems on chip (SoCs). These analog data bring new challenges to design engineers. How do we translate all those analog senses we use everyday into the world of digital and back again? The answer lies in analog and digital converters.

There's good reason why analog IC design is often considered to be more of an art than a science. Traditionally, analog functionality commonly resided on a single, discrete chip. Now, with changes in technology and a broadening use of analog solutions, the trend is towards integrated, mixed-signal SoCs. Yet, compared to their digital counterparts, analog components are much more susceptible to noise, distortion, and other errors.

Design engineers accustomed to developing analog designs for simple, low-end products often find that their familiar design techniques aren't effective on high-end applications. Significant technical adjustments are needed. After all, supporting the latest communications and sensor interfaces calls for high-performance data converters and analog front ends (AFEs),

sensors, clocks and other timing solutions, and power regulators. Developing these IP blocks carries some unique design challenges. Here, we outline five key challenges to be aware of when designing analog systems for high-end applications:

- Sampling rates
- Bit resolution
- Noise ratio
- Effective number of bits (ENOB)
- Power

Table 1 outlines optimal resolution and sampling rate ranges for key wireless and Internet of Things applications.

Application	Resolution (bits)	Speed
Measurement	16–18	1KSPS
Audio	16–24	48, 96, 192KSPS
Monitoring/touch	10–12	1–2MSPS
WIFI IQ	10	80/160MSPS
LTE IQ	12	62/125MSPS

Table 1: Optimal resolution and sampling rates for key applications

Sampling Rates: How Fast Can You Go?

If you can remember back to your college courses, you might recall something about a funny theorem by Nyquist. (Didn't think you would ever have to recall that again, huh?) According to the Nyquist sampling theorem, to generate an accurate reproduction of an analog signal in digital form, the sampling rate should be higher than twice the highest frequency of the signal.[1] The faster the speed in sampling incoming or outgoing data in a data converter, the more accurate the rendition of analog signals. However, faster sampling speeds call for higher bandwidth, which consumes more power and requires better synchronization between multiple bits. What's more, synchronization at higher speeds—3Gbps or more—becomes more difficult.

Consider, as an example, a 7-bit analog-to-digital converter (ADC). An ADC calls for seven individual sample sizes, which means each sample must be synchronized in order to sample at the right timing. At higher speeds, this synchronization proves quite challenging. By contrast, for low-end design, one can have multiple analog-to-digital (A to D) sampling points across fewer bits, so synchronization is less of a concern. Ultimately, determining the optimal sampling rate is not simply about getting to the fastest rate. See Figure 1 for a look at ideal sampling rates and resolution for high-end application areas.

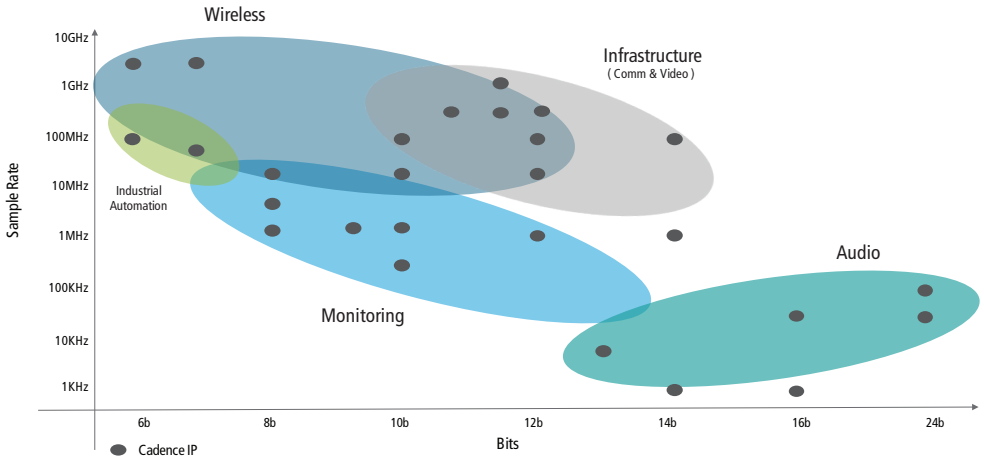

Figure 1: A look at sampling rates and bits for high-end applications

Bit Resolutions: How Accurate Do You Need to Be?

Bit resolution is a reflection of how closely we can represent the analog signal as a digital value. If you are an audiophile, you hear talk about bit resolution all the time, especially disagreements about whether digital is as good as old-fashioned tubes (analog). A data converter's resolution conveys how many discrete values it can produce over the range of analog values.

So, the real question is, how accurately do you need to represent the analog signal? In an application such as audio, designers desire a higher bit resolution because our ears are very sensitive to changes and variations. By contrast, in applications such as temperature sensors in a home environment, where the variation in temperature is less critical, one can use a lower number of bits.

From a practical standpoint, the "useful" resolution of a converter is limited by the best signal-to-noise ratio (SNR) that the converter can achieve for a digitized signal.[2] All designers must take these tradeoffs into consideration when selecting the right ADC/digital-to-audio converter (DAC).

Noise Ratio: How Much Noise Can Your Design Tolerate?

When considering the noise ratio, it is all a matter of the application. In application designs such as wireless speakers, it seems obvious that any noise added to the original signal impacts the performance and quality of the experience. When you are listening to music, you don't want to hear the squelch or static that noise causes.

In the conversion of analog signals, any noise will reduce the accuracy of the digital representation. For example, there might be noise from other signals in the circuitry, which reduces the accuracy of the data converter signal. So, a design engineer must consider placement of neighboring components and circuitry on the chip in order to achieve an optimal SNR. Expressed in bits, the resolution tells the engineer the maximum possible average SNR for an ideal ADC without oversampling.

So, applications such as wireless speakers cannot tolerate a lot of noise, while applications such as temperature sensors can tolerate a greater range of noise. The design engineer must determine the need for greater margins such as higher bit rate or faster sampling rate to accommodate for the SNR.

ENOB: What Does the Performance Really Look Like?

Effective number of bits (ENOB) is a comprehensive way to measure the overall A to D performance. In a 7-bit ADC application, for example, it might be impossible to get good performance up to seven bits resolution due to noise and distortion. For example, an ENOB of six or higher for a 7-bit ADC reflects a well-optimized design, but an ENOB of five or lower for the same ADC indicates an ADC more susceptible to noise and environmental conditions.

The ENOB value takes into consideration the impact of noise, distortion, variations, and temperature on the performance of the converter. However, it's important to gauge what the quality of the A to D conversion will be like in a real application, when factors such as signals, noise, and temperature are considered. Essentially, one should strive to have an ENOB that is as high as the number of bits in the ADC.

Another consideration is that the ENOB value can help to determine the specification for your ADC, which might not be obvious at first evaluation. As an example, an 11-bit ADC with an ENOB of 10.5 might be more effective in your design than a 12-bit ADC with an ENOB of 10. This incongruity highlights the importance of understanding the system requirements rather than just a specific feature of a converter.

Power: What is the Ideal Mix with Amplitude?

In all designs today, power continues to be a concern. With the move to include analog circuitry into mobile applications, power has become an increasingly critical concern. The perception has always been that analog is a power hog; however, the reality is that the only true power concern is on the transmit side (DAC).

With the DAC at higher rates, there's concern about how big of an amplitude of the signal to drive, but power becomes a tradeoff: higher amplitude means more power consumption. The challenge is to achieve high amplitude without sacrificing power. Consider a signal at 2V with a 1ms time frame and a 10 milliamp drive. What if you reduced the time frame to drive the signal higher? At 1/2ms with the same conditions, you would need to double-correct to accurately drive the signal.

Conclusion: A Faster Design Cycle with Ready-to-Use IP Blocks

As this paper has outlined, there are several key challenges to address when designing with analog. Given the fast time-to-market, product performance, and product differentiation pressures faced by today's designers, proven and ready-to-use IP blocks present an efficient option. Cadence offers a broad portfolio of more than 250 hardened, tested, and silicon-proven analog IP blocks that are ready to integrate into designs.

The IP family, supporting 28nm designs, provides a conversion rate that's up to 10X faster compared to competing solutions and includes a 7-bit 3GSPS dual ADC and DAC, an 11-bit 1.5GSPS dual ADC, and a 12-bit 2GSPS dual DAC. The data converter IP cores can be integrated into a complete AFE. Using these analog IP blocks, design engineers can focus on developing unique features and functions for their SoC, rather than worrying about noise, synchronization, layout, and other issues.

Footnotes

1. Source: http://en.wikipedia.org/wiki/Analog-to-digital_converter

2. Source: http://en.wikipedia.org/wiki/Analog-to-digital_converter

For Further Information

To learn more about off-the-shelf analog IP, visit: http://www.cadence.com/cadence/newsroom/features/Pages/AnalogIP.aspx

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