

# Watchdog Timer (WDT) IP

## Overview

**Cadence® IP Factory** delivers custom, synthesizable IP to support specific design requirements.

The **Cadence Watchdog Timer IP** is compliant with the *AMBA® 2 Specification*.

The **Cadence Watchdog Timer IP** is a 15-bit hardware countdown timer with prescaler that can be used to recover from system lockup, such as when software is trapped in a deadlock.

The **Cadence Watchdog Timer IP** is architected to quickly and easily integrate into any system-on-chip (SoC) that supports an ARM® AMBA® 2 Advanced Peripheral Bus (APB).

The **Cadence Watchdog Timer IP** provides a convenient, cost-effective solution for watchdog fault detection in your design. It offers SoC integrators the advanced capabilities and support that not only meet, but exceed the requirements of high-performance designs and implementations.

**Cadence SoC Peripheral IP** is silicon proven and has been extensively validated with multiple hardware platforms.

**Cadence IP Factory** offers comprehensive IP solutions that are in volume production, and have been successfully implemented in more than 400 applications.

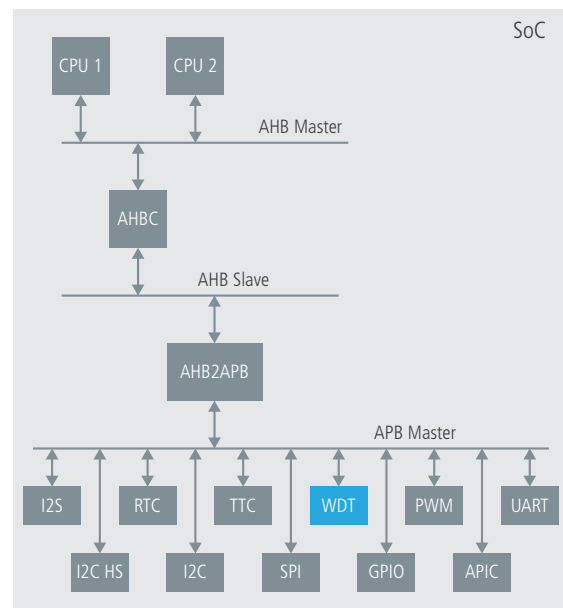


Figure 1: Example System-level Block Diagram

## Key Features

- System reset, interrupt request, and external signal outputs
- Time out range of 32,760 to 268,431,360 clock cycles
- Variable output pulse width, programmable for each output independently
- Counter access and restart keys prevent unintended changes to the counter value and restart state
- All registers are accessible through the APB interface
- APB slave interface to SoC

## Product Details

The **Cadence Watchdog Timer IP** provides software deadlock detection and fault recovery for ARM-based SoC designs.

## Period Counter

The Period Counter consists of a programmable 15-bit countdown timer with prescaler. Time out ranges of 32,760 to 268,431,360 clock cycles (derived from pclk on the APB interface) are possible.

The Period Counter reload value and prescaler are written to a single Counter Control register to simplify **Cadence Watchdog Timer IP** configuration. An access key is provided in the register to prevent unintended changes to the reload and prescaler values.

In normal operation, the **Cadence Watchdog Timer IP** is restarted before the counter value reaches zero, thus preventing the **Cadence Watchdog Timer IP** from generating an output signal. Like the Counter Control register, a key is used to write the restart value, thus preventing anomalous software operation from interfering with **Cadence Watchdog Timer IP** operation.

The status of the **Cadence Watchdog Timer IP** can be read at any time to determine if a time out event has occurred.

## Output and Input Signals

The **Cadence Watchdog Timer IP** has three separate outputs, system reset (wd\_rst\_n), interrupt request (wd\_irq), and external zero request (ex\_wdz\_n), for indicating a time out event has occurred. Outputs can be individually enabled or disabled.

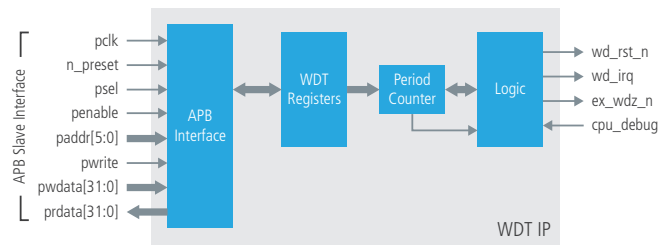


Figure 2: IP-level Block Diagram

The length of the pulse for each output is independently programmable.

The **Cadence Watchdog Timer IP** also has an input (cpu\_debug) for stopping the Period Counter when the CPU is stopped in delay mode.

## Signal Interface

The **Cadence Watchdog Timer IP** supports an APB slave interface for connection to APB bus masters such as a CPU core, or AHB2APB bridge. The APB slave interface includes PSEL and PENABLE, allowing a single SoC to contain multiple peripherals.

## Cadence IP Factory

**Cadence IP Factory** can deliver various configurations of SoC Peripheral IP to meet your design requirements.

For more information, visit [ip.cadence.com](http://ip.cadence.com)

## Benefits

- Low-risk solution—silicon-proven design
- Ease-of-use—customizable with easy integration
- Easy integration—supports industry-standard APB interface

## Related Products

- Triple Timer Counter (TTC) IP

## Deliverables

- Clean, readable, synthesizable Verilog HDL
- Cadence Encounter® RTL Compiler synthesis scripts
- Documentation – integration and user guide, release notes
- Sample verification testbench

## Available Products

- Watchdog Timer (WDT) IP



Cadence Design Systems enables global electronic design innovation and plays an essential role in the creation of today's electronics. Customers use Cadence software, hardware, IP, and expertise to design and verify today's mobile, cloud, and connectivity applications. [www.cadence.com](http://www.cadence.com)

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