

Universal Asynchronous Receiver Transmitter (UART) IP

Overview

Cadence® IP Factory delivers custom, synthesizable IP to support specific design requirements.

The **Universal Asynchronous Receiver Transmitter IP** is compliant with the *AMBA® 2 Specification*.

The **Universal Asynchronous Receiver Transmitter IP** provides full duplex operation with configurable FIFOs on both transmit and receive. A modem interface is provided allowing connection to many popular modem devices.

The **Universal Asynchronous Receiver Transmitter IP** provides a cost-effective solution for demanding applications. It offers system-on-chip (SoC) integrators the advanced capabilities and support that not only meet, but exceed the requirements of high-performance designs and implementations.

The **Universal Asynchronous Receiver Transmitter IP** is architected to quickly and easily integrate into any SoC that supports an ARM® AMBA® 2 Advanced Peripheral Bus (APB).

Cadence SoC Peripheral IP is silicon proven, with a 10-year history of reliable design-ins, and has been extensively validated with multiple hardware platforms.

Cadence IP Factory offers comprehensive IP solutions that are in volume production, and have been successfully implemented in more than 400 applications.

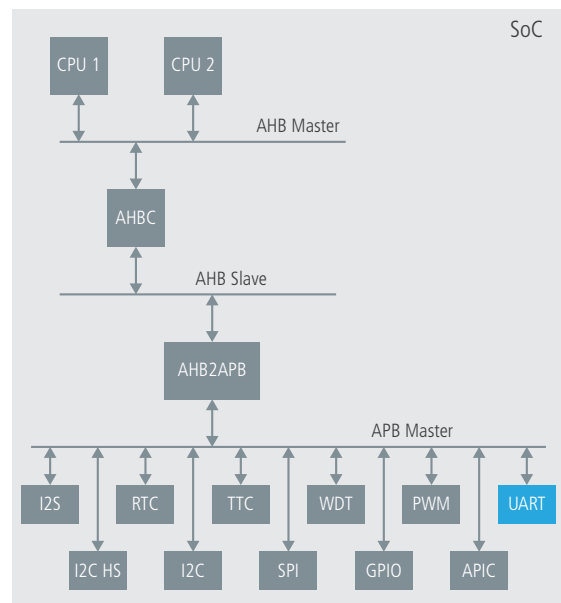


Figure 1: Example System-level Block Diagram

Key Features

- Compliant with AMBA 2 Specification
- Programmable baud rate from 110bps to 115.2kbps
- Supports 6, 7, and 8 data bits on serial input and output with 1, 1.5, or 2 stop bits
- Modem control interface with CTS, RTS, DSR, DTR, RI, and DCD signals
- Parity, framing, and overflow error detection
- Provides bidirectional IrDA 1.4 interface
- Supports 8-, 16-, or 32-bit wide APB slave interface
- Loopback capabilities include local, remote, and automatic echo modes

Product Details

The **Universal Asynchronous Receiver Transmitter IP** full-duplex, serial operation at bit rates up to 115kbps.

Control Logic

The control logic provides all the necessary logic for managing the components that make up the **Universal Asynchronous Receiver Transmitter IP**. It also contains a full set of configuration registers for defining the UART IP operation.

All registers are accessed through the APB interface.

Interrupt Handler

The **Universal Asynchronous Receiver Transmitter IP** can be programmed to generate an interrupt on one of several different event types. Supported event types include empty and full FIFO conditions, line break and parity errors. Interrupts can be individually enabled, disabled, and masked. The interrupt handler generates a single interrupt request from all interrupt sources.

Software can get information about the interrupt source, and clear the interrupt, through the APB Interface.

FIFO Monitor Interface

The FIFO monitor interface provides separate outputs for monitoring the state of the receive and transmit FIFOs. Each FIFO has full, empty, and threshold trigger status outputs. In addition, the transmit FIFO has a “near full” status output.

Modem Control Interface

The modem control interface provides handshake signals for controlling typical modem devices. Six active-low signals, CTS, RTS, DSR, DTR, RI, and DCD, are provided.

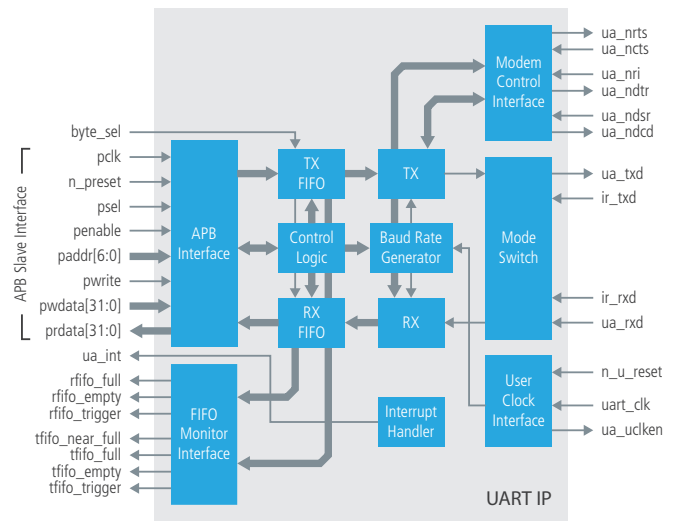


Figure 2: IP-level Block Diagram

Mode Switch and IrDA Interface

The mode switch provides serial outputs for connection to a modem, or IrDA 1.4-compliant transceiver, at speeds up to 115.2kbps.

APB Interface

Target applications access the **Universal Asynchronous Receiver Transmitter IP** through an APB slave interface. The APB Interface can be configured for 8-, 16-, or 32-bit width.

Cadence IP Factory

Cadence IP Factory can deliver various configurations of SoC Peripheral IP to meet your design requirements.

With 10+ years of experience and 400+ successful designs in process nodes ranging from 180nm to 22nm, **Cadence IP Factory** solutions have been proven in everything from low-power MP3 players to leading edge supercomputers.

For more information, visit ip.cadence.com

Benefits

- Low-risk solutions—silicon-proven design
- Fully configurable—FIFO size, bus width, UART operation
- Easy integration—supports industry-standard APB interface

Deliverables

- Clean, readable, synthesizable Verilog HDL
- Cadence Encounter® RTL Compiler synthesis scripts
- Documentation – integration and user guide, release notes
- Sample verification testbench

Available Products

- Universal Asynchronous Receiver Transmitter (UART) IP

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