Overview

**Cadence® IP Factory** delivers custom, synthesizable IP to support specific design requirements.

The **Cadence Triple Timer Counter IP** is compliant with the **AMBA® 2 Specification**.

The **Cadence Triple Timer Counter IP** contains three independently programmable 16-bit timer/counters with 16-bit prescalers. The input to each prescaler/counter pair can be taken from the ARM® AMBA® 2 Advanced Peripheral Bus (APB) interface clock (pclk), or an external clock input (ext_clk[3:1])

The **Cadence Triple Timer Counter IP** is architected to quickly and easily integrate into any system on chip (SoC), and to connect seamlessly to Cadence, or third-party, APB-based bus master devices.

The **Cadence Triple Timer Counter IP** provides a convenient, cost-effective timing solution for your design. It offers SoC integrators the advanced capabilities and support that not only meet, but exceed the requirements of high-performance designs and implementations.

**Cadence SoC Peripheral IP** is silicon proven and has been extensively validated with multiple hardware platforms.

**Cadence IP Factory** offers comprehensive IP solutions that are in volume production, and have been successfully implemented in more than 400 applications.

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**Key Features**

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<th>Feature</th>
<th>Description</th>
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<tr>
<td>Three independent 16-bit timers/counters</td>
<td>Internal (pclk) or external clock source</td>
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<td>Interrupt generated on six different events for each timer/counter</td>
<td>16-bit event timer on each timer/counter for measuring output pulse width</td>
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<td>Each timer/counter supports count up and count down operation</td>
<td>Count register for each timer/counter can be read at any time through the APB interface</td>
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<td>APB slave interface to SoC</td>
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Product Details

The Cadence Triple Timer Counter IP is a low gate count, flexible peripheral for providing advanced timing and counting features to any SoC design.

Timers/Counters

The Cadence Triple Timer Counter IP contains three independent 16-bit timer/counters. Each timer/counter can be clocked from the APB interface (pclk), or a separate external clock input (ext_clk[3:1]). External clock inputs are synchronized to pclk before being applied to the corresponding timer/counter.

Each timer/counter can be configured for count up or count down operation.

Prescaler

Each timer/counter includes a programmable, 16-bit prescaler to decrease the frequency of the clock sent to the timer/counter. Since the prescaler is a simple divider, the input frequency of the timer/counter can be divided by 2 to 65,536.

Event Timer

Each timer/counter has a programmable, 16-bit event timer to measure the pulse width of the corresponding ext_clk input, allowing the Cadence Triple Timer Counter IP to work with noisy signals.

Interrupts

The Cadence Triple Timer Counter IP has three separate interrupt outputs, one for each timer/counter. Individual interrupts can be configured through the APB interface.

Benefits

• Low-risk solution—silicon-proven design
• Ease-of-use—customizable with easy integration
• Easy integration—supports industry-standard APB interface

Deliverables

• Clean, readable, synthesizable Verilog HDL
• Cadence Encounter® RTL Compiler synthesis scripts
• Documentation — integration and user guide, release notes
• Sample verification testbench

Available Products

• Triple Timer Counter (TTC) IP

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