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Systems and Peripherals Datasheet

Pulse Width Modulator (PWM) IP

Overview

Cadence® IP Factory delivers custom, synthesizable IP to support specific design requirements.

The **Cadence Pulse Width Modulator IP** is compliant with the *AMBA® 2 Specification*.

Using a generic design without process-specific elements, the **Cadence Pulse Width Modulator IP** is architected to quickly and easily integrate into any system on chip (SoC), and can be targeted to virtually any technology.

The target application can easily modify the shape of the waveform during operation, adjusting both the period and high time through an ARM® AMBA® 2 Advanced Peripheral Bus (APB) slave interface. The **Cadence Pulse Width Modulator IP** also incorporates all basic functions needed for standalone operation.

The **Cadence Pulse Width Modulator IP** provides a cost-effective solution for demanding applications. It offers SoC integrators the advanced capabilities and support that not only meet, but exceed the requirements of high-performance designs and implementations.

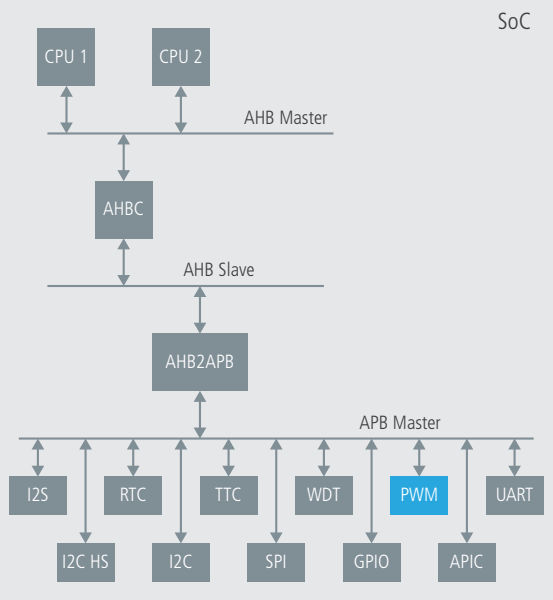

Figure 1: Example System-level Block Diagram

Cadence SoC Peripheral IP is silicon proven, with a 10-year history of reliable design-ins, and has been extensively validated with multiple hardware platforms.

Cadence® IP Factory offers comprehensive IP solutions that are in volume production, and have been successfully implemented in more than 400 applications.

Key Features

- Compliant with AMBA 2 Specification
- Parameterizable address and module ID
- Fully programmable, the shape of the output waveform can be easily modified
- Generates a regular rectangular wave of definable period and duty cycle
- Programmable interrupt for complex waveforms
- APB slave interface for programming PWM registers
- Single clock domain, single edge design

Product Details

The **Cadence Pulse Width Modulator IP** generates a regular rectangular wave of definable period and duty cycle. PWM operation can be started and stopped with a single register write, allowing the **Cadence Pulse Width Modulator IP** to operate indefinitely without target application intervention.

PWM Module

The **Cadence Pulse Width Modulator IP** is fully programmable. The PWM output period and high time (duty cycle) can be modified at any time by the target application.

- The 32-bit period register (PR) controls the PWM output period. Expressed in terms of system clock cycles, the period register is programmable from 2 to 4,294,967,294 ($2^{32} - 2$).
- The 32-bit hightime register (HR) controls the time the PWM output is high. Also expressed in terms of system clock cycles, the hightime register is programmable from 1 to 4,294,967,293 ($2^{32} - 3$).

Subsequent writes to the period and hightime registers take place at the end of the current period.

The control register (CR) starts and stops the PWM Module. When the target application writes a one-bit start value to the control register, the PWM module generates the PWM cycle. Operation continues until the target application writes a one-bit stop value. Once stopped, the PWM output is held high until the next start.

The **Cadence Pulse Width Modulator IP** can generate interrupts every time the period register overflows. Interrupts can be enabled or disabled by writing to the enable interrupt (EI) and disable interrupt (DI) registers, respectively. Pending interrupts are cleared by reading the interrupt status (IS) register. The current state of the EI register can be read from the read interrupt value (RI) register.

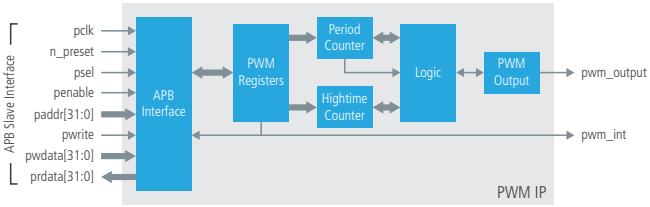

Figure 2: IP-level Block Diagram

The module ID (ID) register is read-only, but parameterizable, allowing your system design to contain more than one **Cadence Pulse Width Modulator IP**.

All registers are accessed through the APB interface.

APB Interface

Target applications access the **Cadence Pulse Width Modulator IP** through an APB slave interface.

APB timings are specified relative to the target clock period and are coded into the provided synthesis script. These timings are for guidance only. The practical maximum clock period depends on system usage requirements and would be the required increment in PWM period and hightime.

Cadence® IP Factory

Cadence IP Factory can deliver various configurations of SoC Peripheral IP to meet your design requirements.

With 10+ years of experience and 400+ successful designs in process nodes ranging from 180nm to 22nm, **Cadence IP Factory** solutions have been proven in everything from low-power MP3 players to leading edge supercomputers.

For more information, visit ip.cadence.com

Benefits

- Low-risk solution—silicon-proven design
- Fully configurable—programmable period and duty cycle
- Easy integration—supports industry-standard APB interface

Related Products

- Real Time Clock (RTC) IP
- Triple Timer Counter (TTC) IP

Deliverables

- Clean, readable, synthesizable Verilog HDL
- Cadence Encounter® RTL Compiler synthesis scripts
- Documentation – integration and user guide, release notes
- Sample verification testbench

Available Products

- Pulse Width Modulator (PWM) IP

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