

General Purpose I/O (GPIO) IP

Overview

Cadence® IP Factory delivers custom, synthesizable IP to support specific design requirements.

The **General Purpose I/O IP** is compliant with the *AMBA® 2 Specification*.

The **General Purpose I/O IP** provides up to 32 I/O ports that can be programmed individually for input, output, or bidirectional operation. Each port can be programmed to trigger the GPIO interrupt on level (high, low) or edge (rising, falling, any) events.

The **General Purpose I/O IP** provides a cost-effective solution for demanding applications. It offers system-on-chip (SoC) integrators the advanced capabilities and support that not only meet, but exceed the requirements of high-performance designs and implementations.

The **General Purpose I/O IP** is architected to quickly and easily integrate into any SoC that supports an ARM® AMBA® 2 Advanced Peripheral Bus (APB).

Cadence SoC Peripheral IP is silicon proven, with a 10-year history of reliable design-ins, and has been extensively validated with multiple hardware platforms.

Cadence IP Factory offers comprehensive IP solutions that are in volume production, and have been successfully implemented in more than 400 applications.

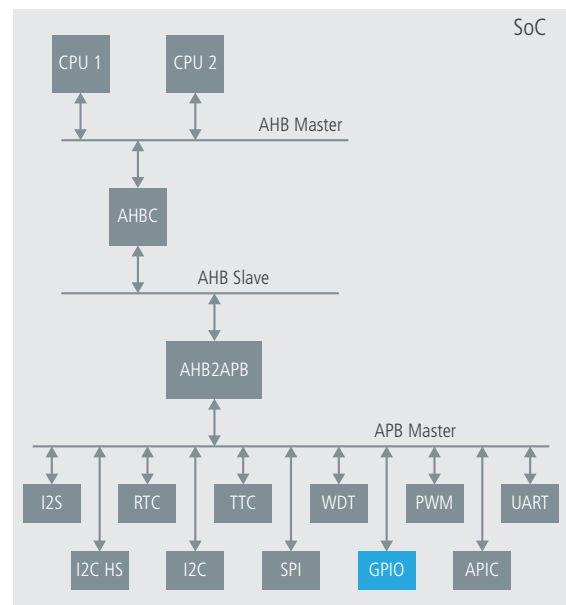


Figure 1: Example System-level Block Diagram

Key Features

- Compliant with AMBA 2 Specification
- Input, output, and output enable for each port
- Bypass interface allows each port to connect directly to a separate peripheral
- 32 ports of input, output, or bidirectional operation
- Programmable interrupt with several event types
- Each port supports input and output registers to latch data to and from the APB slave interface

Product Details

The **General Purpose I/O IP** provides up to 32 ports of general-purpose I/O. Each port can be programmed individually for input, output, or bidirectional operation. The single GPIO interrupt can be programmed to trigger from any, or all, of the GPIO ports.

GPIO Registers

The **General Purpose I/O IP** contains a full set of configuration registers for defining the GPIO IP operation. Input and output registers latch data from the APB slave interface.

All registers are accessed through the APB interface.

Interrupt Handler

Each port can be programmed to generate an interrupt on one of several different event types. Supported event types include high and low level, rising edge, falling edge, and any edge events. Interrupts can be individually enabled, disabled, and masked. The Interrupt Handler generates a single interrupt request from all GPIO ports.

Software can get information about the interrupt source, and clear the interrupt, through the APB interface.

Bypass Interface

The bypass interface provides separate inputs and outputs for directly connecting each GPIO port to different peripherals. Incoming and outgoing data is not latched, so signal levels at the

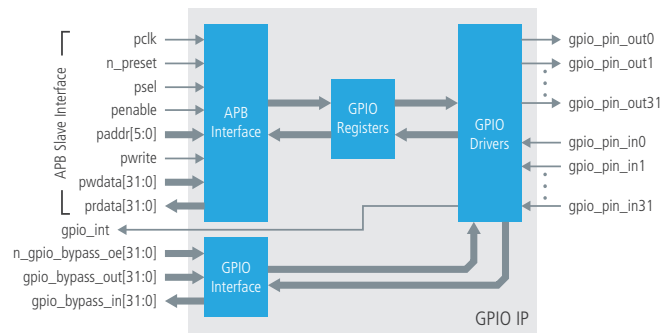


Figure 2: IP-level Block Diagram

bypass interface must be maintained to hold the GPIO port at the correct level.

APB Interface

Target applications access the **General Purpose I/O IP** through an APB slave interface.

Cadence IP Factory

Cadence IP Factory can deliver various configurations of SoC Peripheral IP to meet your design requirements.

With 10+ years of experience and 400+ successful designs in process nodes ranging from 180nm to 22nm, **Cadence IP Factory** solutions have been proven in everything from low-power MP3 players to leading edge supercomputers.

For more information, visit ip.cadence.com

Benefits

- Low-risk solution—silicon-proven design
- Fully configurable—each port is individually programmable
- Easy integration—supports industry-standard APB interface

Deliverables

- Clean, readable, synthesizable Verilog HDL
- Cadence Encounter® RTL Compiler synthesis scripts
- Documentation – integration and user guide, release notes
- Sample verification testbench

Available Products

- General Purpose I/O (GPIO) IP

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