Overview

**Cadence® IP Factory** delivers custom, synthesizable IP to support specific design requirements.

The **Cadence T8051 Microcontroller IP** is compliant with the Intel MCS® 51 instruction set.

The **Cadence T8051 Microcontroller IP** is a low gate count, single-chip 8-bit microcontroller, which provides you with an interface for serial communication, a timer, a debugger, as well as multi-purpose I/O ports and hardware interrupts.

The **Cadence T8051 Microcontroller IP** is architected to quickly and easily integrate into any system-on-chip (SoC), while achieving a very low gate count and effectively sharing a wide range of resources between several stages of instruction execution inside the CPU.

Being easily re-programmable, the **Cadence T8051 Microcontroller IP** is used in situations when the microcontroller should replace hard-coded control logic and enable introducing modifications to the control algorithm without the need to re-design the chip. Complex debugging system implemented is an additional value of the core.

The **Cadence T8051 Microcontroller IP** provides a convenient, cost-effective and low power solution that gives you relatively high performance. A complete OCDS debugging system compatible with the industry-standard Keil™ µVision Cx51 Development Tools IDE is also available.

**Cadence SoC Peripheral IP** is silicon proven and has been extensively validated with multiple hardware platforms.

**Cadence IP Factory** offers comprehensive IP solutions that are in volume production, and have been successfully implemented in more than 400 applications.

**Key Features**

- Compliant with Intel MCS 51 instruction set
- Four priority levels, 11 interrupt sources (80C517-like)
- Input and output ports with single 8-bit I/O port and alternate port functions, 16-bit timer/counter
- Internal data memory interface addressing up to 256B of data memory space
- Full duplex serial interface with 8 or 9-bit UART modes, variable baud rate and a baud rate generator
- External memory interface addressing up to 64kB of external program memory and external data memory
- Eight external interrupts, a complete debugging solution compatible with the 8051 series
- De-multiplexed address/data bus to ease the connection with memories and program memory write mode
Product Details

The **Cadence T8051 Microcontroller IP** is a low gate count microcontroller which can be applied in many various system types, including mixed-signal, low-speed, low-power, or FPGA-based systems.

**CPU (Central Processing Unit)**

Receiving instructions from program memory, the CPU uses RAM or SFRs as operands. It provides the ALU with 8-bit arithmetic, logic, multiplication and division operations, as well as Boolean manipulations.

The RAM and SFR interfaces can address up to 256 bytes of read/write data memory space and built-in or off-core Special Function Registers. The memory interface can address up to 64kB of both program memory and external data memory.

**Port**

The core offers also parallel I/O port controller, which allows the said port to be used with off-core buffers and is fully compatible with the classic 8051.

**Serial 1**

To enable full-duplex communication, a flexible UART port is included. The Serial1 port operates in 8- and 9-bit UART modes and applies variable baud rate, which is generated internally.

**Extint**

Eight external interrupt inputs are samples and edge or level checked thanks to this module. Two interrupts are falling edge or low level sensitive, two are rising or falling edge, and the remaining four are rising-edge sensitive.

**ISR**

An 80C515-compatible interrupt controller with eleven sources and four priority levels is provided, with each source having one or more of its own request flags in a dedicated SFR. Each interrupt requested by the corresponding flag can be individually enabled or disabled by dedicated enable bits in the SFRs.

**PMU**

The PMU serves two power management modes: IDLE and STOP. The IDLE mode leaves the clock for peripherals running, allowing power consumption to drop. With any interrupt or reset, the CPU exits this state. In the STOP Mode, all internal clocks are turned off and the CPU exits this state with a non-clocked external interrupt or reset condition, making internally generated interrupts obsolete.

**OCDS**

The OCDS unit serves as a debug interface through a IEEE1149.1 (JTAG) port. It provides functions such as: run, stop, single-step, hardware and software breakpoints, debugger program execution and read/write access to program memory, external/internal data memory and SFRs.

**Timer 0**

This timer counts external pulses (1 to 0 transitions) on the “t0” pin and operates in four modes: 13- or 16-bit timer/counter, 8-bit timer/counter with auto reload, and dual 8-bit timer.

**Cadence IP Factory**

**Cadence IP Factory** can deliver various configurations of SoC Peripheral IP to meet your design requirements.

For more information, visit [ip.cadence.com](http://ip.cadence.com)

---

**Benefits**

- Low-risk solutions—silicon proven design
- Ease-of-use—customizable with easy integration
- Lowest gate count 8051-compliant architecture

**Related Products**

- EASE-8051 IP

**Deliverables**

- Clean, readable, synthesizable Verilog HDL, VHDL
- Cadence Encounter® RTL Compiler synthesis scripts
- Documentation – integration and user guide, release notes
- Sample verification testbench

**Available Products**

- T8051 Microcontroller IP

Cadence Design Systems enables global electronic design innovation and plays an essential role in the creation of today’s electronics. Customers use Cadence software, hardware, IP, and expertise to design and verify today’s mobile, cloud, and connectivity applications. [www.cadence.com](http://www.cadence.com)