Systems and Peripherals Datasheet

Sony/Philips Digital Interface Controller (S/PDIF) IP

Overview

Cadence® IP Factory delivers custom, synthesizable IP to support specific design requirements.

The **Cadence Sony/Philips Digital Interface Controller IP** is fully compliant with *ARM® AMBA® 2 On-Chip Bus Specification*.

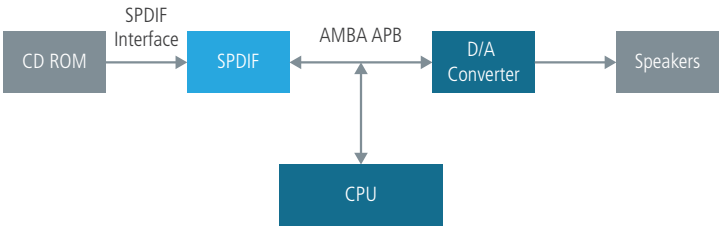

Figure 1: Example System-Level Block Diagram

The **Cadence Sony/Philips Digital Interface Controller IP** is a core that implements the Sony/Philips Digital Interface (IEC 60958), an unidirectional and self-clocking interface for connecting digital audio equipment by using linear and non-linear PCM coded audio samples. The non-linear usage occurs with pass-through supported.

The **Cadence Sony/Philips Digital Interface Controller IP** is architected to quickly and easily integrate into any system-on-chip (SoC) thanks to the adherence to interface standards such as ARM AMBA 2 APB.

The **Cadence Sony/Philips Digital Interface Controller IP** provides a convenient, cost-effective solution and offers advanced configurability thanks to a rich set of parameters which allow easy integration of the core to the user application.

High performance is yet another benefit of the compact architecture offered by the **Cadence Sony/Philips Digital Interface Controller IP**, affecting the silicon size and increasing power saving.

Cadence Systems and Peripherals IP is silicon-proven and has been extensively validated with multiple hardware platforms.

Cadence IP Factory offers comprehensive IP solutions that are in volume production, and have been successfully implemented in more than 400 applications.

Key Features

- Compliant with AMBA 2 On-Chip Bus specification, AMBA APB supported
- Integrated AMBA APB slave wrapper to interface with the APB controller
- Receiver and transmitter modes available
- DMA master handshake interfacing supported
- Data mode capabilities such as: sample rate 3kHz-192kHz and 20/24 bit per sample
- Event stimulated internal interrupt request generation with masking capability
- Synchronization hold in the under-run condition, clock recovery from the SPDIF data stream
- Configurable size of external FIFO (64 words default), 64 to 512 word depth of the FIFO memory
- Sample rate detection from the received data stream
- Direct FIFO interface for reading data from the FIFO (RX mode) or writing data to the FIFO (TX mode)

Product Details

The **Cadence Sony/Philips Digital Interface Controller IP** is a solution that can be used in digital audio, video, and other multimedia systems, in high quality multi channel audio transmission of linear PCM data, as well as in other instances of optical serial communication.

SPDIF TRX

In a given time instant the SPDIF core can act as either transmitter or receiver, but cannot perform both functions in parallel. The SPDIF core is able to synchronize with an input data stream, after reaching synchronization. It also provides the code that indicates detected sample rate of the received data. In order to be able to receive input data correctly, SPDIF receiver requires internal sampling clock of frequency eight times higher than the input data bit rate.

SFR

The SFR is a set of 4 registers that provides status of SPDIF core and FIFO and allow controlling some of their settings. AMBA APB can be accessed only in 32bit bus access mode.

FIFO Controllers

There are two FIFO subcomponents: APB FIFO and SPDIF FIFO.

Working at *pclk* clock domain, the APB FIFO block is responsible for controlling communication between the APB wrapper and the dual-port RAM memory.

Working at *clk_spdif* clock domain, the SPDIF FIFO block is used for controlling communication between the **Cadence Sony/Philips Digital Interface Controller IP** core and the dual-port RAM memory.

Both of these components are provided with interfaces for handling dual-port RAM that stores transmit and receive data.

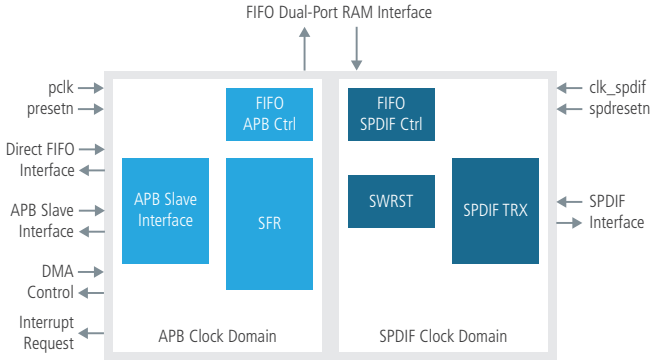

Figure 2: IP-Level Block Diagram

Grey code counter is used for FIFO pointer generation and synchronization between the two mentioned clock domains is done with the aid of Grey-coded addresses.

APB Slave Interface

The APB bus slave wrapper, compatible with AMBA 2 APB Bus Specification, connects the SFR block and the FIFO to the AMBA APB bus. The APB bus slave wrapper implements two APB bus slave interfaces that have separate slave select signals *pselsfr* and *pselfifo*, but share other bus signals.

SWRST

Used for synchronizing purposes only, the SWRST subcomponent ensures software reset signals synchronization in the *clk_spdif* clock domain. The reset signal synchronization is made on the rising edge of the system clock.

Cadence IP Factory

Cadence IP Factory can deliver various configurations of Systems and Peripherals IP to meet your design requirements.

For more information, visit ip.cadence.com

Benefits

- Low-risk solutions—silicon-proven design
- Ease-of-use—customizable with easy integration
- Advanced configurability and a rich set of parameters

Related Products

- I2S Multi-Channel Inter-IC Sound Bus Controller (I2S-MC) IP
- I2S Single Channel Inter-IC Sound Bus Controller (I2S-SC) IP

Deliverables

- Clean, readable, synthesizable Verilog HDL
- Cadence Encounter® RTL Compiler synthesis scripts
- Documentation – user guide, implementation specification, release notes
- Sample verification testbench

Available Products

- Sony/Philips Digital Interface Controller (S/PDIF) IP

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