Systems and Peripherals Datasheet

Inter Integrated Circuit (I2C) IP

Overview

Cadence® IP Factory delivers custom, synthesizable IP to support specific design requirements.

The **Cadence Inter Integrated Circuit IP** is compliant with the *AMBA® 2 APB protocol* and uses the *I2C bus specification version 2.0*.

The **Cadence Inter Integrated Circuit IP** is a bus controller that can function as a master or a slave in a multi-master, two-wire serial I²C bus. In master mode, the I²C interface can transmit data to a slave, as well as initiate transfer to receive data from it.

The **Cadence Inter Integrated Circuit IP** is architected to quickly and easily integrate into any system-on-chip (SoC) and provides a convenient, cost-effective solution by using two sets of signals, one to deal with I/O and another to interface with the AMBA APB bus.

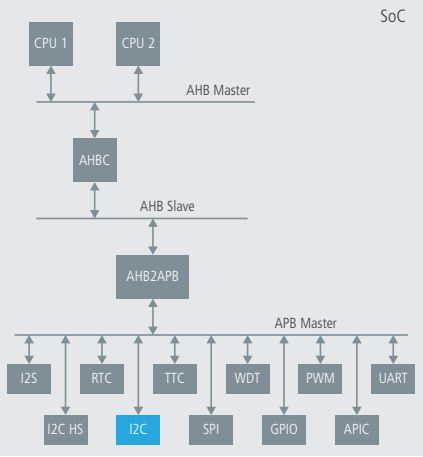

Figure 1: Example System-level Block Diagram

When embedded as a master in a multi-master bus, the **Cadence Inter Integrated Circuit IP** performs arbitration for bus ownership and clock synchronization with other bus masters. This prevents any corruption of data when more than one master tries to transmit or receive data at the same time.

Cadence SoC Peripheral IP is silicon proven and has been extensively validated with multiple hardware platforms.

Cadence IP Factory offers comprehensive IP solutions that are in volume production, and have been successfully implemented in more than 400 applications.

Key Features

- Compliant with AMBA 2 APB protocol and I²C bus specification version 2.0
- Supports normal (100kHz) and fast (400kHz) bus data rates, as well as normal or extended addressing
- Slave monitor in master set up, I²C bus hold for slow host service
- Slave time out detection with programmable period, transfer status interrupts and flags
- Combined format transfers both as master and slave
- System clock speed over 200 MHz
- Clock synchronization and bus arbitration, fully programmable slave response address
- Optional reversible FIFO with parameterizable depth and the same register array for receive and transmit

Product Details

The **Cadence Inter Integrated Circuit IP** is a bus controller programmable as either a master or a slave interface, which can use both normal 7-bit and extended 10-bit addressing modes.

Register type FIFO

Register type FIFO can be optionally implemented in the design. This FIFO is reversible to keep the gate count of the module low with the same FIFO used both for transmit and receive. It is accessed by the host through a single APB register.

In master mode, the FIFO allows the host to load a request for multiple data bytes transfer and receive notification when this request is serviced by the I²C interface, or when the transfer is terminated prematurely due to error or time out. The host can determine the reasons and the outstanding amount of data by reading the interrupt status register and transfer size register.

In slave mode, the FIFO allows for buffering the received data or storing transmit data in advance to reduce the load on the host servicing the I²C interface.

I²C Interface

The I²C interface is capable of holding the I²C bus by keeping the sclk line low until the host provides more data to allow transfer to continue, or until the host allows the transfer to be terminated. If bus hold mode is not activated by the host, the interface terminates the transfer when acting as master.

In the slave mode, it allows the transfer to be terminated after the amount of data provided by the host is transferred.

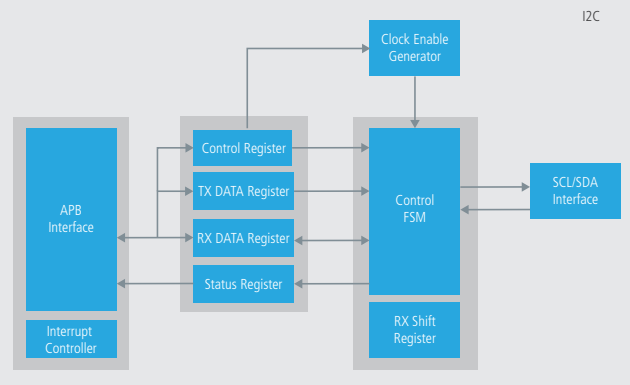

Figure 2: Example IP-level Block Diagram

In either of the mentioned modes, the I²C interface is capable of detecting excessively long periods of the sclk signal being low on the bus which is signified by a maskable interrupt. The time out period is programmable by the host.

When set up as master, the I²C module can be driven in slave monitor mode. While in it, an attempt is made to access a slave so as to check if that slave is ready to respond and perform a transfer.

Cadence IP Factory

Cadence IP Factory can deliver various configurations of SoC Peripheral IP to meet your design requirements.

For more information, visit ip.cadence.com

Benefits

- Low-risk solutions—Silicon-proven design
- Ease-of-use—customizable with easy integration
- High configurability and industry-standard interfaces supported

Related Products

- I2C High-Speed Bus Controller (I2C-HS) IP

Deliverables

- Clean, readable, synthesizable Verilog HDL
- Cadence Encounter® RTL Compiler synthesis scripts
- Documentation – integration and user guide, release notes
- Sample verification testbench

Available Products

- Inter Integrated Circuit (I2C) IP

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