Overview

Cadence® IP Factory delivers custom, synthesizable IP to support specific design requirements.

The Cadence Inter Integrated Circuit IP is compliant with the AMBA® 2 APB protocol and uses the I²C bus specification version 2.0.

The Cadence Inter Integrated Circuit IP is a bus controller that can function as a master or a slave in a multi-master, two-wire serial I²C bus. In master mode, the I²C interface can transmit data to a slave, as well as initiate transfer to receive data from it.

The Cadence Inter Integrated Circuit IP is architected to quickly and easily integrate into any system-on-chip (SoC) and provides a convenient, cost-effective solution by using two sets of signals, one to deal with I/O and another to interface with the AMBA APB bus.

When embedded as a master in a multi-master bus, the Cadence Inter Integrated Circuit IP performs arbitration for bus ownership and clock synchronization with other bus masters. This prevents any corruption of data when more than one master tries to transmit or receive data at the same time.

Cadence SoC Peripheral IP is silicon proven and has been extensively validated with multiple hardware platforms.

Cadence IP Factory offers comprehensive IP solutions that are in volume production, and have been successfully implemented in more than 400 applications.

Key Features

- Compliant with AMBA 2 APB protocol and I²C bus specification version 2.0
- Supports normal (100kHz) and fast (400kHz) bus data rates, as well as normal or extended addressing
- Slave monitor in master set up, I²C bus hold for slow host service
- Slave time out detection with programmable period, transfer status interrupts and flags
- Combined format transfers both as master and slave
- System clock speed over 200 MHz
- Clock synchronization and bus arbitration, fully programmable slave response address
- Optional reversible FIFO with parameterizable depth and the same register array for receive and transmit
Product Details

The Cadence Inter Integrated Circuit IP is a bus controller programmable as either a master or a slave interface, which can use both normal 7-bit and extended 10-bit addressing modes.

Register type FIFO

Register type FIFO can be optionally implemented in the design. This FIFO is reversible to keep the gate count of the module low with the same FIFO used both for transmit and receive. It is accessed by the host through a single APB register.

In master mode, the FIFO allows the host to load a request for multiple data bytes transfer and receive notification when this request is serviced by the I2C interface, or when the transfer is terminated prematurely due to error or time out. The host can determine the reasons and the outstanding amount of data by reading the interrupt status register and transfer size register.

In slave mode, the FIFO allows for buffering the received data or storing transmit data in advance to reduce the load on the host servicing the I2C interface.

I2C Interface

The I2C interface is capable of holding the I2C bus by keeping the sclk line low until the host provides more data to allow transfer to continue, or until the host allows the transfer to be terminated. If bus hold mode is not activated by the host, the interface terminates the transfer when acting as master.

In the slave mode, it allows the transfer to be terminated after the amount of data provided by the host is transferred.

Benefits

- Low-risk solutions—Silicon-proven design
- Ease-of-use—customizable with easy integration
- High configurability and industry-standard interfaces supported

Related Products

- I2C High-Speed Bus Controller (I2C-HS) IP

Deliverables

- Clean, readable, synthesizable Verilog HDL
- Cadence Encounter® RTL Compiler synthesis scripts
- Documentation – integration and user guide, release notes
- Sample verification testbench

Available Products

- Inter Integrated Circuit (I2C) IP

Cadence Design Systems enables global electronic design innovation and plays an essential role in the creation of today’s electronics. Customers use Cadence software, hardware, IP, and expertise to design and verify today’s mobile, cloud, and connectivity applications. [www.cadence.com](http://www.cadence.com)

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