cadence®

Systems and Peripherals Datasheet

I2S Single Channel Inter-IC Sound Bus Controller (I2S-SC) IP

Overview

Cadence® IP Factory delivers custom, synthesizable IP to support specific design requirements.

The **Cadence I2S Single Channel Inter-IC Sound Bus Controller IP** is compliant with *Philips® Inter-IC Sound Bus Specification* and *AMBA® 2 APB Specification*.

The **Cadence I2S Single Channel Inter-IC Sound Bus Controller IP** is a configurable single-channel Inter-IC Sound (I²S) bus interface controller that combines functions of a half-duplex transmission mode transmitter and receiver, and a full-duplex transmission mode transceiver.

The **Cadence I2S Single Channel Inter-IC Sound Bus Controller IP** is a microcode-free design that can be targeted at ASIC and FPGA implementations. By supporting additional features of transmission parameters configurable through SFR registers, the **Cadence I2S Single Channel Inter-IC Sound Bus Controller IP** extends the functionality of the core beyond the I²S standard.

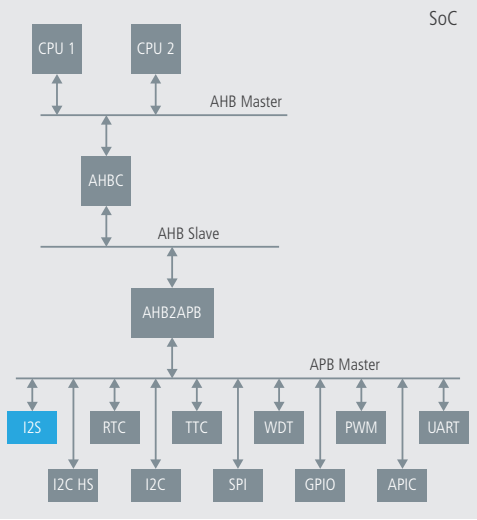

Figure 1: Example System-Level Block Diagram

The **Cadence I2S Single Channel Inter-IC Sound Bus Controller IP** is architected to quickly and easily integrate into any system-on-chip (SoC), and to connect seamlessly to Cadence, or third-party, APB-compliant bus master devices, and I²S devices.

Cadence Systems and Peripherals IP is silicon-proven and has been extensively validated with multiple hardware platforms.

Cadence IP Factory offers comprehensive IP solutions that are in volume production, and have been successfully implemented in more than 400 applications.

Key Features

- Compliant with Philips Inter-IC Sound Bus Specification and ARM AMBA 2 Specification
- Supports I²S transmit, receive, full-duplex, Philips, left-justified, right-justified, DSP, and TDM modes
- Internal, event-stimulated interrupt request generation with masking capability
- Continued transmitting after transmitter underrun
- Two configurable internal FIFO buffers for transmitted and received data
- A set of SCK (SCLK) and WS (LRCLK) strobes, handshake interface to external DMA modules
- Wide-configurable stereo channel with up to 16 optional channels that are TDM-supported
- Power saving capability

Product Details

The **Cadence I2S Single Channel Inter-IC Sound Bus Controller IP** is a configurable single-channel Inter-IC Sound (I²S) bus interface controller that combines functions of both transmitter and receiver.

TRX Controller with TX Data and RX Data

The TRX controller module is a common controller for I²S data processing modules–the TX Data and RX Data modules.

FIFO Controllers

Each of two FIFO controllers contains two instantiations of FIFO control unit. These controllers provide proper synchronization between two clock domains (clk_hst for APB side FIFO control units and clk for I²S transceiver side FIFO control unit) with the aid of Grey-coded addresses.

SFR

The host clock domain Special Function Registers (SFR) subcomponent is a set of fourteen registers that provide status information for the **Cadence I2S Single Channel Inter-IC Sound Bus Controller IP** and FIFO components, while also handling their settings configuration.

APB Slave Interface

With 32-bit data buses, the APB slave interface provides access to Special Function Registers and transmission FIFO memories.

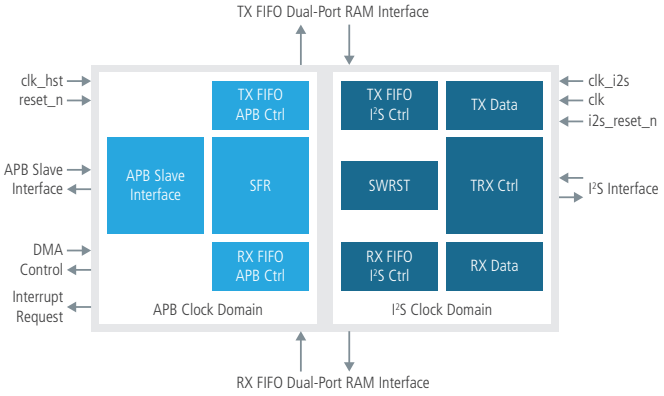

Figure 2: IP-Level Block Diagram

SWRST

Used for synchronizing purposes only, the SWRST subcomponent ensures software reset signals synchronization between two clock domains (I²S and APB). The reset signal synchronization is made on rising edge of the system clock.

Cadence IP Factory

Cadence IP Factory can deliver various configurations of Systems and Peripherals IP to meet your design requirements.

For more information, visit ip.cadence.com

Benefits

- Low-risk solutions—silicon-proven design
- Ease-of-use—customizable with easy integration
- Easy integration—supports industry-standard ARM AMBA APB interface

Related Products

- I2S Multi-Channel Inter-IC Sound Bus Controller (I2S-MC) IP

Deliverables

- Clean, readable, synthesizable Verilog HDL
- Cadence Encounter® RTL Compiler synthesis scripts
- Documentation – user guide, implementation specification, release notes
- Sample verification testbench

Available Products

- I2S Single Channel Inter-IC Sound Bus Controller (I2S-SC) IP

cadence®

Cadence Design Systems enables global electronic design innovation and plays an essential role in the creation of today's electronics. Customers use Cadence software, hardware, IP, and expertise to design and verify today's mobile, cloud, and connectivity applications. **www.cadence.com**

V2.3 06/15, IP no. IP6716E