cadence®

Systems and Peripherals Datasheet

I2S Multi-Channel Inter-IC Sound Bus Controller (I2S-MC) IP

Overview

Cadence® IP Factory delivers custom, synthesizable IP to support specific design requirements.

The **Cadence Multi-Channel Inter-IC Sound Bus Controller IP** is compliant with *Philips® Inter-IC Sound Bus Specification* and *AMBA® 2 APB Specification*.

The **Cadence Multi-Channel Inter-IC Sound Bus Controller IP** is a stereo audio transmission core with a wide spectrum of applications in connecting digital and audio devices.

Combining the functions of a transmitter and a receiver, the **Cadence Multi-Channel Inter-IC Sound Bus Controller IP** can be targeted at ASIC and FPGA implementations.

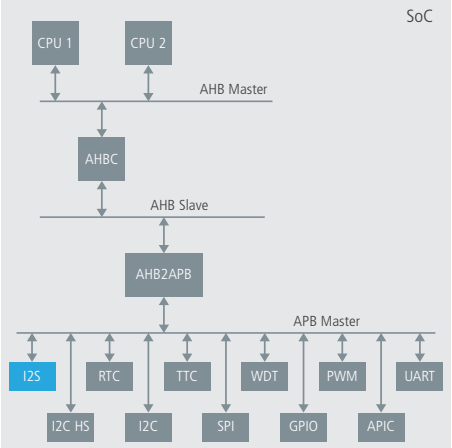

Figure 1: Example System-Level Block Diagram

The **Cadence Multi-Channel Inter-IC Sound Bus Controller IP** is architected to quickly and easily integrate into any system-on-chip (SoC). For seamless integration of the core in AMBA-based microprocessors, additional elements are provided, including ARM® AMBA® APB slave interface, transmit and receive FIFO control units, SFR block, and eight I²S channels .

The **Cadence Multi-Channel Inter-IC Sound Bus Controller IP** provides a convenient, cost-effective solution with advanced configurability and multi-channel connection support. Configurable features include the depth of external Transmit and Receive FIFO, 16 to 65,536-words each (with a 16-words default value).

Cadence Systems and Peripherals IP is silicon-proven and has been extensively validated with multiple hardware platforms. **Cadence IP Factory** offers comprehensive IP solutions that are in volume production, and have been successfully implemented in more than 400 applications.

Key Features

- Compliant with Philips Inter-IC Sound Bus Specification and ARM AMBA 2 Specification
- Supports I²S Philips, left-justified, right-justified, DSP, and user modes
- ARM AMBA APB bus slave interface for data and programming, two FIFO buffers supported
- Continued transmitting after transmitter underrun
- Two clock domains (APB for the host side clock domain and system clock for the I²S channels)
- Two sets of SCK (SCLK) and WS (LRCLK) strobes, one configuration register block for all channels
- Interrupts driven by the I²S bus activity events, handshake interface to external DMA modules
- Power-saving capability and eight configurable stereo channels

Product Details

The **Cadence Multi-Channel Inter-IC Sound Bus Controller IP** is a core which combines transmitter and receiver functions for a variety of different applications, such as connecting Analog-to-Digital and Digital-to-Analog converters with very low jitter, error correction for compact disc and digital recording, or digital signal processing.

Moreover, the **Cadence Multi-Channel Inter-IC Sound Bus Controller IP** can be used in ASIC and SoC applications which require multiple channel audio data transmission, as well as in multimedia systems in general.

TRX MC

Meeting the *Philips Inter-IC Sound Bus Specification* requirements, the TRX MC block implements eight channels that can be configured as a transmitter or a receiver, in both master and slave modes. The eight-channel I²S controller is composed of eight transmitter/receiver units and two additional transmit and receive control units.

Figure 2 presents clk_* which denotes ten clocks (from clk_0 to clk_7, clk_rs, and clk_ts). These clocks can be externally gated using strobe signals generated by the **Cadence Multi-Channel Inter-IC Sound Bus Controller IP**.

APB Slave Interface

Compatible with *ARM AMBA 2 APB Bus Specification*, the APB Slave Interface implements two APB slaves that have separate slave select signals and share all other bus signals.

Special Functions Registers

The Special Function Registers (SFR) block is a set of programming registers that enable programming the I²S mode and the FIFO controller settings, while it also provides the I2S-MC and FIFO status. These registers can be accessed only in 32-bit bus mode.

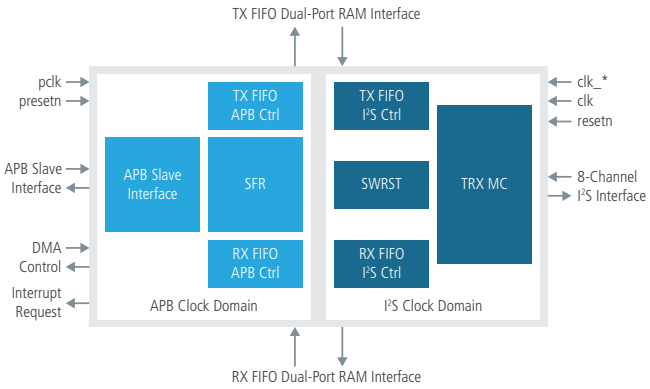

Figure 2: IP-Level Block Diagram

FIFO Controllers

The **Cadence Multi-Channel Inter-IC Sound Bus Controller IP** has two FIFO controllers, one for Transmit and the other one for Receive FIFO. Both controllers contain two FIFO control unit instantiations and provide proper synchronization between two clock domains with the aid of Grey-encoded addresses.

SWRST

Used for synchronizing purposes, the SWRST subcomponent ensures software reset signals synchronization between two clock domains (system clock domain and host clock domain) with the software reset signal synchronization made on the rising edge of the system clock.

Cadence IP Factory

Cadence IP Factory can deliver various configurations of Systems and Peripherals IP to meet your design requirements.

For more information, visit ip.cadence.com

Benefits

- Low-risk solutions—silicon-proven design
- Ease-of-use—customizable with easy integration
- Advanced configurability and multi-channel connection support

Related Products

- Sony/Philips Digital Interface Controller (S/PDIF) IP
- I2S Single Channel Inter-IC Sound Bus Controller (I2S-SC) IP

Deliverables

- Clean, readable, synthesizable Verilog HDL
- Cadence Encounter® RTL Compiler synthesis scripts
- Documentation – user guide, implementation specification, release notes
- Sample verification testbench

Available Products

- I2S Multi-Channel Inter-IC Sound Bus Controller (I2S-MC) IP

cadence®

Cadence Design Systems enables global electronic design innovation and plays an essential role in the creation of today's electronics. Customers use Cadence software, hardware, IP, and expertise to design and verify today's mobile, cloud, and connectivity applications. **www.cadence.com**

V2.3 06/15, IP no. IP6718E