Systems and Peripherals Datasheet

32-bit APB Serial Peripheral Interface (SPI) IP

Overview

Cadence® IP Factory delivers custom, synthesizable IP to support specific design requirements.

The **Cadence 32-bit APB Serial Peripheral Interface IP** is compliant with *AMBA® 2 Specification* Revision.

The **Cadence 32-bit Serial Peripheral Interface IP** is a full-duplex, synchronous, four-wire, serial bus interface compliant with many existing SPI designs.

Supporting both master and slave interfaces, the **Cadence 32-bit APB Serial Peripheral Interface IP** operates in single, and multi-master environments. FIFO depth and width is configurable to support virtually any protocol and throughput requirements.

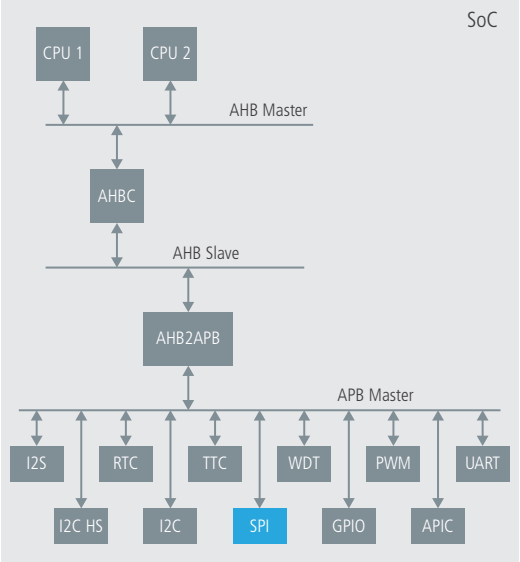

Figure 1: Example System-level Block Diagram

The **Cadence 32-bit APB Serial Peripheral Interface IP** is architected to quickly and easily integrate into any SoC, and to connect seamlessly to Cadence, or third-party, APB-compliant bus master devices, and SPI peripherals.

The **Cadence 32-bit APB Serial Peripheral Interface IP** provides a convenient, cost-effective connection between your SoC and external SPI peripherals. It offers SoC integrators the advanced capabilities and support that not only meet, but exceed the requirements of high-performance designs and implementations.

Cadence SoC Peripheral IP is silicon proven and has been extensively validated with multiple hardware platforms.

Cadence IP Factory offers comprehensive IP solutions that are in volume production, and have been successfully implemented in more than 400 applications.

Key Features

- Full-duplex operation, simultaneous receive and transmit
- Separate transmit and receive FIFOs
- Operates in master or slave mode
- ARM® AMBA® APB slave interface to SoC
- Supports up to four external peripherals in master mode
- Optional reference clock input block
- Programmable master mode clock frequencies

Product Details

The **Cadence 32-bit APB Serial Peripheral Interface IP** interfaces CPU cores and other on-chip APB master devices to a broad range of off-chip SPI peripherals.

SPI Master Interface

The SPI Master Interface module handles all bit operations directly at the SPI bus level, freeing the application processor for other tasks while SPI communication is ongoing. In master mode, the SPI Master Interface provides serial output, serial input, the SPI clock, and slave select signals.

In multi-master environments, the SPI Master Interface can detect if more than one master is active at a time, and signal an error to the application processor.

SPI Slave Interface

Like the SPI Master Interface, the SPI Slave Interface module handles all bit operations directly at the SPI bus level. The interrupt can be programmed to signal a start condition.

Transmit and Receive FIFOs

The **Cadence 32-bit APB Serial Peripheral Interface IP** contains separate transmit and receive FIFOs. FIFO width and depth can be configured for each FIFO independently at compile time.

SPI Clock Generation

The SPI clock on the SPI Master Interface can be driven from the APB interface, an external clock source, or the optional reference clock module, allowing for up to a 1:1 pclk to sclk_out ratio. The **Cadence 32-bit APB Serial Peripheral Interface IP** supports both positive and negative clock polarities.

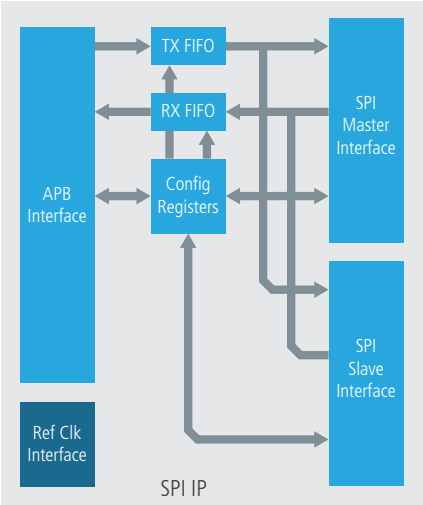

Figure 2: IP-level Block Diagram

Serial clock generation is disabled when the **Cadence 32-bit APB Serial Peripheral Interface IP** is in slave mode.

Signal Interface

The **Cadence 32-bit APB Serial Peripheral Interface IP** supports an APB Slave interface for connection to APB bus masters such as a CPU core, or AHB2APB bridge. A programmable interrupt is also provided to alert the APB bus master of exceptional situations. The APB Slave interface includes PSEL and PENABLE, allowing a single SoC to contain multiple **Cadence 32-bit APB Serial Peripheral Interface IPs**.

Cadence IP Factory

Cadence IP Factory can deliver various configurations of SoC Peripheral IP to meet your design requirements.

For more information, visit ip.cadence.com

Benefits

- Low-risk solutions—silicon proven design
- Ease-of-use—customizable with easy integration
- Easy integration—supports industry-standard APB interface

Related Products

- I2C High-Speed Bus Controller (I2C-HS) IP
- Inter Integrated Circuit (I2C) IP
- 8-bit SFR Serial Peripheral Interface IP

Deliverables

- Clean, readable, synthesizable Verilog HDL
- Cadence Encounter® RTL Compiler synthesis scripts
- Documentation – integration and user guide, release notes
- Sample verification testbench

Available Products

- 32-bit APB Serial Peripheral Interface (SPI) IP

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V2.2 06/14