The Cadence® Tensilica® Imaging/Video product line delivers high performance and power efficiency for today’s demanding imaging and video applications.

IVP and IVP-EP are embedded processors that establish a new standard in high-performance, low-power digital signal processing (DSP) cores specifically designed for image and video processing.

IVP and IVP-EP architecture provides advanced VLIW/SIMD support for the industry’s highest number of ALU operations per processor cycle, as well as a very wide memory bandwidth, to allow for sufficient pixel processing throughput.

IVP is the baseline VLIW/SIMD imaging and video DSP core with specialized instructions to efficiently speed up pixel processing. These instructions were optimized in close collaboration with a number of customer and partner companies.

IVP-EP offers up to 4X the performance compared to IVP.

IVP and IVP-EP are suitable for mobile imaging as well as consumer (DTV, gaming) and automotive vision applications.

Each embedded processor is delivered as either a complete subsystem or a user-generated processor core.

The Tensilica Imaging/Video product line provides unprecedented flexibility in system implementations at power-consumption levels that significantly reduce the need for hardware accelerators.

**Benefits**

- IVP and IVP-EP are high-performance, energy-efficient imaging/video embedded processors
- IVP-EP has up to 4X higher performance for application processing with 8b and mix of 8b/16b data compared to flagship IVP, as well as other optimized features for high performance
- Complete subsystem solution, ready to drop into SoC designs
- Customized for better code density, fewer cycles, and lower power
- Significant performance boost for both image/video pixel filtering, as well as computer vision algorithms requiring extensive frame analysis
- Sustained power-efficient video or burst-image processing
- Comprehensive software toolsuite for implementing high-performance imaging pipelines
- Instruction-set extensibility, allowing headroom for improved performance
- Optimized performance and power for computer vision and pixel processing applications that span a large range of data types from 8b to 32b, such as face detection, object detection, lens distortion correction, and many more advanced applications

**Toolchain**

The IVP and IVP-EP processors are delivered with a complete set of software tools. The toolset includes a high-performance C/ C++ compiler with automatic vectorization to support the VLIW pipeline in the IVP-EP core.
This comprehensive toolset also includes the linker, assembler, debugger, profiler, and graphical visualization tools.

A comprehensive instruction set simulator (ISS) allows you to quickly simulate and evaluate performance. When working with large systems or lengthy test vectors, the fast, functional TurboXim™ simulator option achieves speeds that are 40X to 80X faster than the ISS for efficient software development and functional verification.

Tensilica XTensa® Modeling Protocol (XTMP) for system modeling in C and XTensa SystemC (XTSC) for system modeling in SystemC can aid in full-chip simulations. Pin-level XTSC offers co-simulation of SystemC and RTL-level offload accelerator blocks for fast, cycle-accurate simulations.

All major back-end EDA flows are supported.