Overview

**Cadence® IP Factory** delivers custom, synthesizable IP to support specific design requirements.

**Cadence LDO Voltage Regulator IP** provides high performance voltage regulation with a low dropout (LDO) voltage in a variety of popular processes.

Low quiescent current improves system efficiency, and Standby mode reduces power dissipation even further, making **Cadence LDO Voltage Regulator IP** perfect for handheld applications.

**Cadence LDO Voltage Regulator IP** has excellent DC and transient response and built-in soft start control reduces inrush current when fast startup is not required.

**Cadence IP Factory** offers comprehensive IP solutions that are in volume production, and have been successfully implemented in more than 400 applications.

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**Key Features**

- Variety of output voltages available
- Power down capability and low power operation
- Input supply range: 2.0V – 3.3V
- Low quiescent current
- Output currents up to 250mA
- Current limited output
Product Details

Cadence LDO Voltage Regulator IP is characterized by high performance and improved system efficiency, which makes it an ideal solution for power islanding application in digital SoCs.

Architecture

The innovative architecture of Cadence LDO Voltage Regulator IP provides a stable output voltage while consuming low quiescent current, even at output currents as high as 250mA. An available Power-On Reset (POR) output feature provides a digital output indicating the output voltage is stable.

Current Changes and Limits

Cadence LDO Voltage Regulator IP features fast transient response for improved line and load regulation under fast load-current changes.

The current limit feature provided in Cadence LDO Voltage Regulator IP helps reduce inrush current under startup conditions. As the load current exceeds the current limit setting, especially in short circuit conditions, the output voltage starts to fall in order to reduce the power dissipation.

In Standby mode, output current is limited to a much lower value.

Cadence IP Factory

Cadence IP Factory can deliver various configurations of Analog Power IP to meet your design requirements.

For more information, visit ip.cadence.com

Available Products

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Process</th>
<th>Input Voltage Range (V)</th>
<th>Output Voltage Range (V)</th>
<th>Output Current (mA)</th>
<th>Current Limit (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>IP9327C</td>
<td>TSMC 40LP</td>
<td>2.0 – 3.3</td>
<td>1.4 – 2.5</td>
<td>150</td>
<td>200</td>
</tr>
<tr>
<td>IP9333C</td>
<td>TSMC 65LP</td>
<td>2.0 – 3.3</td>
<td>0.8 – 1.4</td>
<td>50</td>
<td>100</td>
</tr>
<tr>
<td>IP9337C</td>
<td>TSMC 65LP</td>
<td>2.0 – 3.3</td>
<td>1.5 – 3.0</td>
<td>250</td>
<td>400</td>
</tr>
</tbody>
</table>

Benefits

• Ease of use—easy SoC integration
• Power-efficient—power down capability
• High performance—improved efficiency

Deliverables

• FE views—Layout exchange format (LEF), .lib file, Verilog
• GDSII, netlist (SPICE format for Cadence Assura® Layout vs. Schematic Verifier (LVS))
• Footprint (LEF)
• User documentation, integration guidelines, engineering datasheet
• Silicon validation report (where available)

Figure 2: IP-Level Block Diagram