

# Design IP for USB 3.0 xHCI Host Controller

## Overview

For over two decades, the Universal Serial Bus interface has truly lived up to its name - it has become the versatile connection standard that is present in a majority of electronic devices - laptops, mobile phones, portable electronics. After years of industry ubiquity of USB 2.0, USB 3.0 applications are becoming the preferred option due to close to 10x better performance to handle the growth of data that is being transferred between devices.

Compliant with Universal Serial Bus 3.0 Specification, Revision 1.0 and xHCI Specification, Revision 1.0, the Cadence® Design IP for USB 3.0 xHCI Host Controller operates in SuperSpeed (5Gbps), High-Speed (480Mbps), Full-Speed (12Mbps), and Low-Speed (1.5 Mbps) modes. The PHY interface complies with USB PHY Interface for PCI Express® (PIPE) for USB 3.0, as well as USB 2.0 Transceiver Macrocell Interface (UTMI+) Specification.

Combined with the Cadence PHY IP for USB Type-C™ designs, the Controller IP provides a complete solution for the next generation of USB applications that will make use of the new, flexible USB Type-C connector.

The Controller IP is architected to quickly and easily integrate into any system on chip (SoC) as an integrated solution with any Cadence or third party USB PHY IP. Host applications access the controller through the industry- standard AMBA® AXI system bus with an optional PCIe® interface.

The Controller IP is part of the comprehensive Cadence Design IP portfolio comprised of Interface, Memory, Analog, and Systems and Peripherals IP.

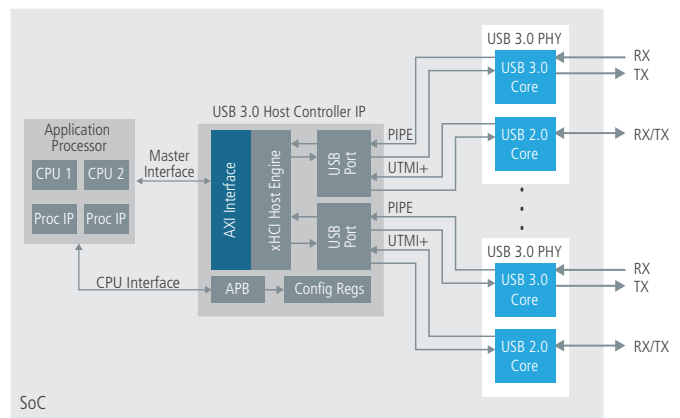


Figure 1: Example System-Level Block Diagram

## Benefits

- **Support for all USB speeds—connect to every USB device**
- **Industry-standard interfaces—simple system integration**
- **Available as integrated solution—less time spent on verification**

## Key Features

- SuperSpeed (5Gbps), High-Speed (480Mbps), Full-Speed (12Mbps), and Low Speed (1.5 Mbps) modes of operation
- AXI4 Master system bus interface with support AXI4 features
- Compliant with USB 3.0 and xHCI specifications
- PIPE interface for USB 3.0 and UTMI+ for USB 2.0
- Configurable number of USB 2.0 and USB 3.0 ports
- Ready for integrated delivery with the Cadence USB PHY IP

## Product Details

The Controller IP is aimed at providing SoC designers with the most robust way to implement a USB interface in their applications.

## System Interface

The Controller IP features a 64-bit data/address AXI Master interface and a 32-bit data/address APB Slave interface. The AXI Master interface provides support for outstanding and out of order transactions.

Both AXI Master and APB Slave interfaces can operate at variety of frequencies to adjust to customer's application. Range of frequencies supported depends on the target SoC technology.

## xHCI Host Engine

The xHCI Host Engine implements the DMA engine as defined by the xHCI specification. It uses a command ring to manage both xHC and all attached devices. Interrupts are realized through an event ring, which is handled by the xHCI Host Engine. The DMA engine of the xHCI Host Engine realizes transactions related with both command and event rings management.

Total count of supported devices influences the size of memory implemented in the xHCI Host Engine.

## Root Hub

The root hub implements two separate data paths for USB 3.0 and USB 2.0, respectively. It routes packets between USB ports and the xHCI Host module.

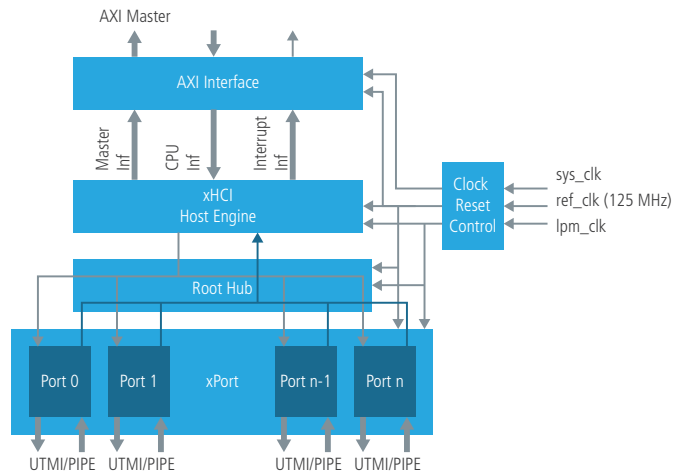


Figure 2: IP-Level Block Diagram

## Root Ports (xPort)

The Controller IP connects to Cadence or third party USB PHYs through the PIPE and UTM/PIPE interfaces for USB 3.0 and 2.0 speeds.

## Availability

The Controller IP is available with support for the following protocol:

Protocol	Speed	Process node
USB 3.0	5Gbps	All

## Related Products

- Cadence PHY IP for USB 3.0
- Cadence PHY IP for USB Type-C
- Cadence Design IP for USB Type-C Port Controller
- Cadence Verification IP for USB Protocols

## Deliverables

- Synthesizable RTL
- Delivery Testbench
- Synthesis and simulation support files
- Documentation

For more information, visit [ip.cadence.com](http://ip.cadence.com)

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