VIP for PCI Express Protocols
Industry-leading verification solutions, proven on hundreds of production designs

Overview
Cadence provides mature and comprehensive Verification IP (VIP) for PCI Express® (PCIe®) protocols. Our VIP run on all major simulators and supports SystemVerilog and other verification languages along with associated methodologies, including the Universal Verification Methodology (UVM). Incorporating the latest protocol updates, each VIP provides a complete bus functional model (BFM), integrated automatic protocol checks, coverage model, and compliance tests. Designed for easy integration in testbenches at IP, system-on-chip (SoC), and system levels, Cadence® VIP for PCIe protocols help you reduce time to first test, accelerate verification closure, and ensure end-product quality.

One-Stop Shop for All PCIe Interfaces
As an active member of the PCI-SIG for many years, Cadence has participated in the development of the PCIe specifications, contributing to the working groups by adding the clarification needed to make the specifications more verifiable.

Cadence has provided pre-silicon VIP for the various PCIe specifications, and worked with dozens of customers worldwide that have used Cadence VIP to verify hundreds of production designs incorporating the range of PCIe interfaces.

Cadence has close partnerships with the main PCI-SIG members, resulting in advanced and proven VIP that follow the latest specification features and revisions. With Cadence, you have a one-stop shop for all PCIe interfaces for testing and verification, with a consistent user API. Table 1 shows the protocols currently supported by Cadence VIP and the associated specification revision level.

<table>
<thead>
<tr>
<th>PCIe Protocols</th>
<th>Spec Revision</th>
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<tbody>
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<td>PCIe 2.0</td>
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<td>PCIe 3.0</td>
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<td>PCIe 4.0</td>
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<td>PCIe 5.0</td>
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<td>SR-IOV</td>
<td>v1.1</td>
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<tr>
<td>MR-IOV</td>
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Table 1: PCIe protocols supported by Cadence VIP
*This specification is rapidly evolving. The VIP are kept current with the latest specification updates.

“Cadence VIP for PCIe 3.0 has enabled us to thoroughly verify that our designs comply with the PCIe 3.0 specification, and the new PCIe 4.0 product demonstrates the company’s commitment to supporting engineers working with this key protocol. By supporting multiple PCIe configurations, popular verification methodologies, and simulators, Cadence VIP have enabled Ineda to support our diverse product configurations with high-quality SoC and IP verification coverage.”

– Balaji Kanigicherla, founder, CTO and vice president of Engineering for Ineda Systems
**Simulation VIP**

The Simulation VIP are ready-made for your environment, providing consistent results whether you are using Cadence or third-party simulators. You have the freedom to build your testbench using any of these verification languages: SystemVerilog, e, Verilog, VHDL, or C/C++. Cadence Simulation VIP supports the UVM as well as legacy methodologies.

The Simulation VIP provide testing for all PCIe components including:

- Root Complex
- Endpoint
- Legacy EP
- Switch

And provides support for all PCIe interfaces including:

- Serial
- PIPE (1.0, 2.0, 3.0, 4.4.1, 5.2)
- 10b/8b
- PIE8
- Transaction-level

**Simulation VIP for PCIe 5.0**

- Operates at 32GT/s
- EIEOS changes for PCIe 5.0
- TS1 and TS2 OS changes for PCIe 5.0
- Equalization bypass capability
- Precoding support
- Supports both PIPE 5.x and serial interfaces
- PIPE SerDes support

**Simulation VIP for PCIe 4.0**

- Built on top of the mature VIP for PCIe 3.0
- Supports speed negotiation and operation at 16GT/s
- Verifies equalization procedure at 16GT/s
- Supports inferring EI for 16GT/s
- Support all PCIe 3.0 ECNs
- Supported for Serial and PIPE interfaces

**Simulation VIP for PCIe 3.0**

- Provides a complete PCIe protocol hierarchy enumeration process including resource allocation
- Provides comprehensive 128/130b encoding scheme checks
- Supports full power management
- Supports D-states, L-states, ASPM
- Supports DC balance testing
- Enables error injection at each layer
- Provides complete link training status state
- Machine (LTSSM) modeling
- Provides comprehensive flow control testing

**Simulation VIP for PCIe 1.1/2.0**

- Supports speed negotiation and link width up-configuration
- Provides user-defined or random lane-to-lane skew insertion
- Supports independent RX clock recovery from incoming bit-stream
- Simulates any link configuration without testbench modification (disabling lanes, inverting lanes, reversing lanes, or changing the allowed link widths)
- Supports end-to-end CRC (ECRC) checking and generation
- Supports automatic transaction ordering rules

**VIP for Single-Root IOV**

- Supports SR-IOV capable endpoint with modeling for physical functions (PFs) and virtual functions (VFs)
- Provides SR-IOV extended capability register modeling
- Supports PF and VF configuration space
- Provides VF BAR and memory request handling
- Supports PF and VF FLR/reset
- Supports PCIM (separate SI support) for RC

**Simulation VIP for Multi-Root IOV**

- Provides MR-IOV extended capability support
- Supports virtual link (VL) testing
- Supports TLP prefix tagging generation
- Supports global key testing
- Provides per-VH reset tests

**Simulation VIP for NVMe 1.3**

- Host and device verification
- Standalone over PCIe and over Arm® AMBA® AXI interface support
- Full support of admin and NVM command set
- Configurable I/O queues
- PRP
- SGL
- Full interrupt support (pin based, MSI, MSI-X)
- CMB and HMB
- Virtualization support

“\nWe’ve determined that 90% of the risk is in chip interfaces. If we design the interfaces incorrectly, it doesn’t matter if we get the rest of the chip right. This is especially true with PCI Express since it’s such a complex protocol. The bottom line for us is that the choice we made to go with proven IP that’s easy to get up and running is really just good, solid common sense.”

– Jim O’Connor, Vice President of Engineering, iVivity
“Wipro has been consistently enabling semiconductor companies to reduce verification time and increase coverage parameters through its next-generation frameworks and market-proven end-to-end verification services. Our partnership with Cadence has played an instrumental role in fulfilling the IP verification needs of our customers. We chose the VIP for PCIe 3.0 along with TripleCheck by Cadence to achieve a comprehensive solution that gives us the fastest path to IP verification closure.”

– A. Vasudevan, VP Semiconductor and Systems, Wipro

**PCle Triplecheck**

**TestSuite**

The TripleCheck™ tool provides an extensive library of compliance tests that are easy to implement. The quick bring-up reduces time-to-first-test and the large test suite provides extensive compliance testing.

Each test is designed to cover specific compliance checklist items, and each test includes a detailed description of purpose, assumptions, scenario, and expected results. Tests are driven from the VIP across the protocol interface toward the design under test, or can be initiated from the application interface of the design.

The testsuite includes thousands of pre-built tests for all protocol layers, state machines and error recovery.

**Functional Coverage**

TripleCheck coverage models support both SystemVerilog and Verification languages. These pre-defined coverage models capture all appropriate data to track and measure verification progress. Open and documented, the models can be extended with application-specific coverage definitions.

**Verification Plan**

TripleCheck provides a verification plan (vPlan) that mirrors the PCIe specification. All requirements in the protocol specification are listed in the vPlan and organized into the same hierarchy as the specification. The vPlan is linked to the coverage model so that coverage data captured during simulation is automatically mapped against the plan. The vPlan also displays progress toward verification closure.

**Accelerated VIP**

Simulating big designs requires hardware-assisted verification, an approach that uses special-purpose hardware, such as Cadence Palladium® XP systems, to dramatically boost simulation performance.

Just as Simulation VIP simplify traditional logic simulation, Accelerated VIP make hardware-assisted verification easier and more productive.

These Accelerated VIP protocols feature Embedded Testbench mode, which supports:

- Descriptor-based programming model
- Scalable internal memory for program and local data
- AMBA AHB slave interface providing full register access and internal memory access
- DMA and DMA scatter-gather capabilities via AMBA AHB master interface
- Configurable hardware and software start/stop conditions
- IRQ with maskable interrupt status registers

**Accelerated VIP for PCIe 2.0/3.0**

- Supports 8/16/32-bit PIPE interface
- Supports serial interface
- All transactions are fully supported
- Up to 8 lanes configuration
- Provides power management testing
- Provides complete set of configuration/status registers
- Provides log transactions in log file + logging control
- Supports 2.5/5/8 GT/s speeds
- Supports link equalization
- Provides backdoor memory access (read/write to own memory)
- Provides stimulus access to received transactions using callbacks
- Provides events to control timing of transactions (reduces HW/SW syncs and gives control to stimulus)
- Supports single root I/O virtualization (SR-IOV)