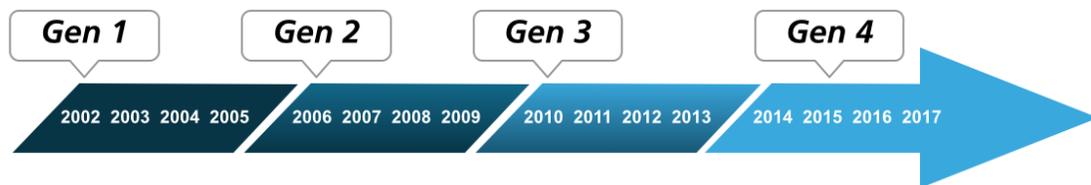


# Cadence VIP for PCI Express Protocols

Industry-leading verification solution, proven on hundreds of production designs

## Overview

Cadence® provides mature and comprehensive verification IP (VIP) for PCI Express (PCIe) protocols. Our VIP runs on all major simulators and supports SystemVerilog and e verification languages along with associated methodologies, including the Universal Verification Methodology (UVM). Incorporating the latest protocol updates, each VIP provides a complete bus functional model (BFM), integrated automatic protocol checks, coverage model, and compliance tests. Designed for easy integration in testbenches at IP, system-on-chip (SoC), and system levels, Cadence VIP for PCIe protocols help you reduce time to first test, accelerate verification closure, and ensure end-product quality.



## One Stop Shop for All PCIe Interfaces

As an active member of the PCI-SIG for many years, Cadence has participated in the development of the PCIe specifications, contributing to the working groups by adding the clarification needed to make the specifications more verifiable.

Cadence has provided pre-silicon VIP for the various PCIe specifications, and worked with dozens of customers worldwide that have used Cadence VIP to verify hundreds production designs incorporating the range of PCIe interfaces.

Cadence has close partnerships with the main PCI-SIG members, resulting in advanced and proven VIP that follows the latest specification features and revisions. With Cadence, you have a one-stop shop for all PCIe interfaces for testing and verification, with a consistent user API. Table 1 shows the protocols currently supported by Cadence VIP and the associated specification revision level.

PCIe Protocols	
Protocol	Specification
PCIe Gen2	v2.1
PCIe Gen3	v3.0
PCIe Gen4	*
NVMe	v1.1
M-PCIe	v1.0
SR-IOV	v1.1
MR-IOV	v1.0

**Table 1: PCIe protocols supported by Cadence VIP**

\*This specification is rapidly evolving. The VIP is kept current with the latest specification updates.

*“Cadence PCIe 3.0 Verification IP has enabled us to thoroughly verify that our designs comply with the PCIe 3.0 specification, and the new PCIe 4.0 product demonstrates the company’s commitment to supporting engineers working with this key protocol. By supporting multiple PCIe configurations, popular verification methodologies and simulators, Cadence VIP has enabled Ineda to support our diverse product configurations with high-quality SoC and IP verification coverage.”*

*– Balaji Kanigicherla, founder, CTO and vice president of Engineering for Ineda Systems*

## Simulation VIP

The Simulation VIP is ready-made for your environment, providing consistent results whether you are using Cadence Incisive®, Synopsys VCS®, or Mentor Questa® simulators. You have the freedom to build your testbench using any of these verification languages: SystemVerilog, e, Verilog, VHDL, or C/C++. Cadence Simulation VIP supports the Universal Verification Methodology (UVM) as well as legacy methodologies.

The PCIe Simulation VIP Provides testing for all PCIe components including:

- Root Complex
- End Point
- Legacy EP
- Switch

And provides support for all PCIe interfaces including:

- Serial
- PIPE (1.0, 2.0, 3.0, 4.3)
- 10b/8b
- PIE8
- Transaction-level

### PCIe 4.0 Simulation VIP

- Built on top of the mature PCIe 3.0 VIP
- Supports Speed negotiation and operation at 16GT/s
- Verifies Equalization procedure at 16GT/s
- Supports Inferring EI for 16GT/s
- Support all PCIe 3.0 ECNs
- Supported for Serial and PIPE Interfaces

### PCIe 3.0 Simulation VIP

- Provides a complete PCI Express protocol hierarchy enumeration process including resource allocation
- Provides comprehensive 128/130b encoding scheme checks
- Supports full power management
- Support (D-states, L-states, ASPM)
- Supports DC Balance testing
- Enables error injection at each layer
- Provides complete link training status state
- Machine (LTSSM) modeling
- Provides comprehensive flow control testing

### PCIe 1.1/2.0 Simulation VIP

- Supports Speed negotiation and link width up-configuration
- Provides User-defined or random lane-to-lane skew insertion
- Supports Independent RX clock recovery from incoming bit-stream

- Simulate any link configuration without
- Testbench modification (disabling lanes,
- Inverting lanes, reversing lanes, or
- Changing the allowed link widths)
- Supports End-to-end CRC (ECRC) checking and generation
- Supports Automatic transaction ordering rules

### Single Root IOV VIP

- Supports SR-IOV capable Endpoint with physical functions (PFs) and virtual functions (VFs) modeling
- Provides SR-IOV extended capability registers modeling
- Supports PF and VF configuration space
- Provides VF BARs and memory requests handling
- Supports PF and VF FLR/reset
- Supports PCIM (separate SI support) for RC

### Multi-Root IOV Simulation VIP

- Provides MR-IOV extended capability support
- Supports Virtual link (VL) testing
- Supports TLP prefix tagging generation
- Supports Global key testing
- Provides Per-VH reset tests

### M-PCIe Simulation VIP

- Provides the mature PCIe VIP API on top of M-PHY
- Supports RMMI and DpDn interfaces
- Supports all High Speed burst gears(HS-G1/HS-G2/HS-G3) and date rate series(A/B)
- Supports Low Speed burst mode called Pulse Width modulation(PWM-G1)
- Supports remote register access protocol (RRAP)
- Supports Asymmetric lane support
- Supports Low power states

### NVM Simulation VIP

- Provides testing for NVMe host and controller
- Built on top of the mature PCIe 3.0 VIP
- Supports Configurable number of I/O queues up to the maximum of 64k
- Supports up to 256 functions 0 physical (PF) or virtual (VF)
- Provides Full support of the admin command and NVM command sets
- Supports PRP Entry and List
- Provides full support of memory-mapped NVMe registers
- Supports end-to-end data protection

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*“M-PCIe helps boost mobile device performance by delivering best-in-class, highly scalable I/O functionality, enabling the migration of business apps to smartphones and tablets as they take on the role of primary computing devices. We are delighted that Cadence is enabling SoC developers to rapidly adopt M-PCIe by delivering IP and VIP products supporting this standard.”*

*– Al Yanes, Chairman and President, PCI-SIG*

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*“Wipro has been consistently enabling semiconductor companies to reduce verification time and increase coverage parameters through its next-generation frameworks and market-proven end-to-end verification services. Our partnership with Cadence has played an instrumental role in fulfilling the IP verification needs of our customers. We chose PCIe Gen3 VIP along with TripleCheck by Cadence to achieve a comprehensive solution that gives us the fastest path to IP verification closure.”*

– A. Vasudevan, VP Semiconductor and Systems, Wipro

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## PCIe Triplecheck

### TestSuite

TripleCheck provides an extensive library of compliance tests that are easy to implement. The quick bring-up reduces time-to-first-test and the large test suite provides extensive compliance testing.

Each test is designed to cover specific compliance checklist items, and each test includes a detailed description of purpose, assumptions, scenario, and expected results. Tests are driven from the VIP across the protocol interface toward the design under test, or can be initiated from the application interface of the design.

The testsuite includes Thousands of pre-built tests for all protocol layers, state machines and error recovery

### Functional Coverage

TripleCheck coverage models support both SystemVerilog and e verification languages. These pre-defined coverage models capture all appropriate data to track and measure verification progress. Open and documented, the models can be extended with application-specific coverage definitions.

### Verification Plan

TripleCheck provides a verification plan (vPlan) that mirrors the PCIe I specification. All requirements in the protocol specification are listed in the vPlan and organized into the same hierarchy as the specification. The vPlan is linked to the coverage model so that coverage data captured during simulation is automatically mapped against the plan. The vPlan also displays progress toward verification closure.

## Accelerated VIP

Simulating big designs requires hardware-assisted verification, an approach that uses special-purpose hardware, like

Cadence® Palladium® XP systems, to dramatically boost simulation performance.

Just as simulation VIP simplifies traditional logic simulation, accelerated VIP makes hardware-assisted verification easier and more productive.

These Accelerated VIP protocols feature Embedded Testbench mode, which supports:

- Descriptor-based programming model
- Scalable internal memory for program and local data
- AHB slave interface providing full register access and internal memory access
- DMA and DMA scatter-gather capabilities via AHB master interface
- Configurable hardware and software start/stop conditions
- IRQ with maskable interrupt status registers

### PCIe 2.0/3.0 Accelerated VIP

- Supports 8/16/32-bit PIPE interface
- Supports Serial interface
- All Transactions are fully supported
- Up to 8 lanes configuration
- Provides Power management testing
- Provides Complete set of configuration/status registers
- Provides Logs transactions in log file + logging control
- Supports 2.5/5/8 GT/s speeds
- Supports Link equalization
- Provides Backdoor memory access (read/write to own memory)
- Provides Stimulus access to received transactions using callbacks
- Provides Events to control timing of transactions (reduces HW/SW syncs and gives control to stimulus)
- Supports Single root I/O virtualization (SR-IOV)

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*“We’ve determined that 90% of the risk is in chip interfaces. If we design the interfaces incorrectly, it doesn’t matter if we get the rest of the chip right. This is especially true with PCI Express since it’s such a complex protocol. The bottom line for us is that the choice we made to go with proven IP that’s easy to get up and running is really just good, solid common sense.”*

– Jim O’Connor, Vice President of Engineering, iVivity

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Cadence Design Systems enables global electronic design innovation and plays an essential role in the creation of today’s electronics. Customers use Cadence software, hardware, IP, and expertise to design and verify today’s mobile, cloud, and connectivity applications. [www.cadence.com](http://www.cadence.com)

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