

Simulation VIP for PCI Express Gen4

First VIP to provide support for PCIe Gen4

Overview

Cadence® Simulation VIP is the world’s most widely used VIP for digital simulation. Hundreds of customers have used Cadence VIP to verify thousands of designs, from IP blocks to full systems on chip (SoCs).

The Simulation VIP is ready-made for your environment, providing consistent results whether you are using Cadence Incisive®, Synopsys VCS®, or Mentor Questa® simulators. You have the freedom to build your testbench using any of these verification languages: SystemVerilog, e, Verilog, VHDL, or C/C++. Cadence Simulation VIP supports the Universal Verification Methodology (UVM) as well as legacy methodologies.

The unique flexible architecture of Cadence VIP makes this possible. It includes a multi-language testbench interface with full access to the source code to make it easy to integrate VIP with your testbench. Optimized cores for simulation and simulation-acceleration allow you to choose the verification approach that best meets your objectives.

Specification Support

This VIP is compliant with draft 0.7 of PCI Express spec 4.0.

Product Highlights

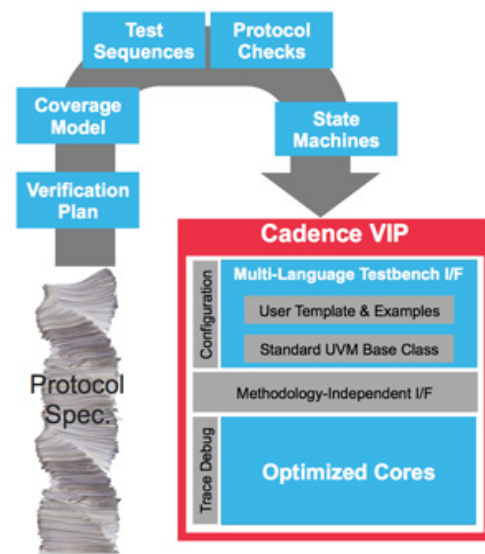
- Provide support for Gen4 equalization testing
- Supports x1, x2, x4, x8, x12, x16, and x32 lanes
- Supports the latest engineering change notices (ECNs)
- Speed negotiation and operation at 16GT/s

Part of a complete PCIe solution including:

- PCIe Gen3
- PCIe Gen2
- NVM Express
- Mobile PCIe
- SR-IOV
- MR-IOV

Supported Design-Under-Test Configurations

- | | | |
|--|---|---|
| <input checked="" type="checkbox"/> Root Complex | <input checked="" type="checkbox"/> End Point | <input checked="" type="checkbox"/> Switch Bridge |
| <input checked="" type="checkbox"/> Full Stack | <input checked="" type="checkbox"/> Controller-only | <input checked="" type="checkbox"/> PHY-only |



Deliverables

People sometimes think of VIP as just a bus functional model (BFM) that responds to interface traffic. But SoC verification requires much more than just a BFM. Cadence Simulation VIP components deliver:

- State machine models incorporate the subtle features of state machine behavior, such as support for multi-tiered, power-saving modes
- Pre-programmed assertions that are built into the VIP to continuously watch simulation traffic to check for protocol violations
- Test suites are provided for most Cadence VIP components
- Pre-programmed coverage models used to capture interesting combinations of simulation results. By analyzing the results collected by the coverage model, engineers can tell if the simulations have exercised the various modes of operation of an interface
- Verification plans for most protocols link the “raw” coverage model results back to the protocol specification

Key Features

- Speed Negotiation at 16GT/s: Full control of the link speed, up and down changes
- Equalization procedure at 16GT/s: Perform and control all equalization aspects
- Inferring EI for 16GT/s: Detecting inferred electrical idle
- Complete link training status state machine (LTSSM) modeling, including all states
- Full support for up and down configuration (link size)
- Adding skew between lanes
- Recover clock from bitstream or use reference clock
- Add jitter to the clock
- Full control of the Ack\Nak protocol and timers, Predefined sequence number, link CRC (LCRC), and duplicate TL errorinjections
- Full control of Flow Control Credits (FCCs), including initial allocation of FCCs and the frequency of on-the-fly FCC updates.
- Serial, 8bit, 10bit, PIPE 3.0, PIPE 4.0, PIE8
- Support for all sidebands: WAKE#, CLKREQ#, PERST#
- End Point, Legacy End Point, Root complex, Bridge, Switch, PHY-DUT
- Complete modeling of 4 address spaces: Memory, I/O, Configuration, MSI\MSI-X
- Automatic, user-defined flow control initialization per virtual channel (VC)
- Full compliance of Function Level Reset
- Full support for the new TS symbols
- Framing Tokens: Error injection, checking, and coverage
- New Skip OS full support
- Protocol multiplexing ECN (Engineering Change Notice)
- Optimized buffer flushfill
- ASPM optionality ECN
- L1 sub states ECN
- Downstream Port Containment ECN
- Lightweight Notification ECN
- PCIe over M-PHY ECN
- Process Address Space ID ECN
- Precision Time Measurement ECN

Test Suite

This VIP includes a basic test suite capability that includes:

- Constrained-random example tests
- 3rd party simulator test execution

Related Products

- PCIe Gen3 Simulation VIP
- PCIe Gen2 Simulation VIP
- PCIe SR-IOV Simulation VIP
- PCIe MR-IOV Simulation VIP
- NVM Express Simulation VIP
- Mobile PCI Simulation VIP
- PCIe Gen2/Gen 3 Accelerated VIP



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