VIP Datasheet

Cadence VIP for MIPI Protocols

Overview

The mature and comprehensive Cadence® Verification IP (VIP) for MIPI® Protocols run on all major simulators and support SystemVerilog and ***e*** Verification languages along with associated methodologies, including the Universal Verification Methodology (UVM). Incorporating the latest protocol updates, each VIP for MIPI protocols provides a complete bus functional model (BFM), integrated automatic protocol checks, coverage model, and compliance tests. Designed for easy integration in testbenches at IP, system-on-chip (SoC), and system levels, the VIP for MIPI protocols help you reduce time to first test, accelerate verification closure, and ensure end-product quality.

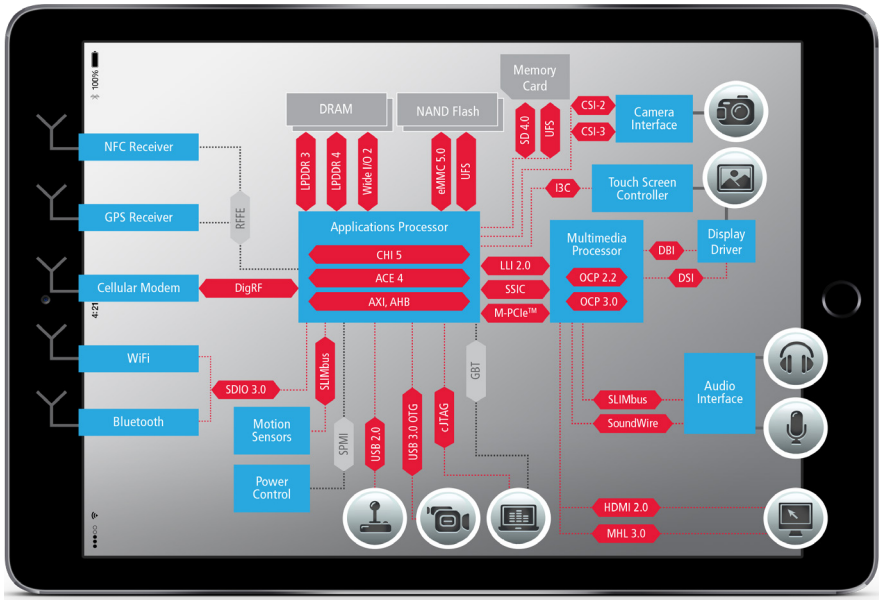


Figure 1: A mobile design example. Cadence provides VIP for all the interfaces shown in red. VIP are also available for these lower-layer MIPI interfaces: C-PHY, D-PHY, M-PHY, and UniPro.

One-Stop Shop for All MIPI Interfaces

As a Contributing Member of the MIPI Alliance since 2007, Cadence has actively participated in the development of the MIPI specifications, contributing to the working groups by adding the clarification needed to make the specifications more verifiable.

Cadence has provided pre-silicon VIP for the different MIPI specifications, and worked with dozens of customers worldwide that have used Cadence VIP to verify over 100 production designs incorporating the different MIPI interfaces.

Cadence has close partnerships with the main MIPI members, resulting in advanced and proven VIP that follow the latest specification features and revisions. With Cadence, you have a one-stop shop for all MIPI interfaces for testing and verification, with a consistent user API. Table 1 shows the protocols currently supported by Cadence VIP and the associated specification revision levels.

Simulation VIP

Cadence Simulation VIP are ready-made for your environment, providing consistent results whether you are using Cadence Incisive®, Cadence Xcelium® or third-party simulators. You have the freedom to build your testbench using any of these verification languages: SystemVerilog, ***e***, Verilog, VHDL, or C/C++. The Simulation VIP supports the Universal Verification Methodology (UVM) as well as legacy methodologies.

Our VIP for MIPI protocols support TripleCheck™ IP Validator, which greatly simplifies and accelerates compliance testing of interface IP.

Simulation VIP for CSI-2

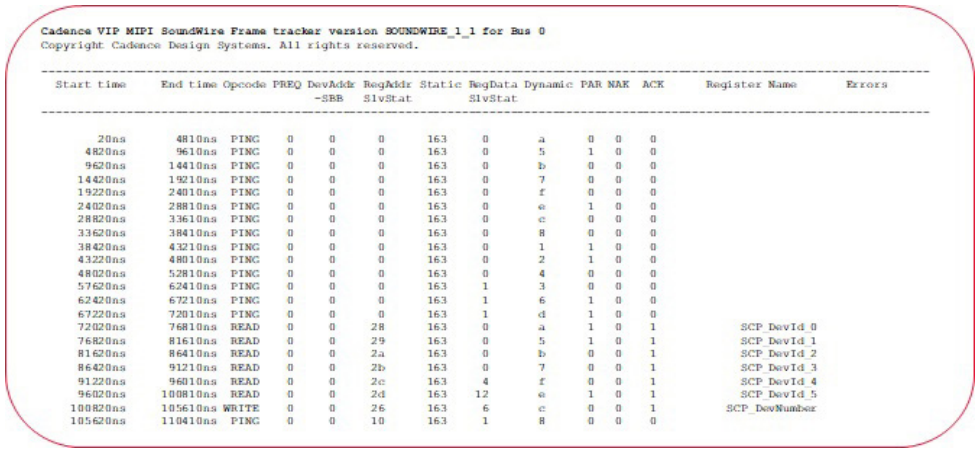
- Used continuously since 2008, and has verified dozens of production designs
- Supports the latest MIPI CSI-2℠ 2.0 specification additions
- Verifies both CSI-2 receiver and transmitter
- Includes VIP for MIPI D-PHY™ and C-PHY™ for physical layer verification
- Provides a comprehensive CSI-2 testsuite, coverage model, and verification plan as part of TripleCheck IP Validator
- Supports Serial and PPI interfaces
- Supports one to four data lanes
- Supports virtual channel and data type interleaving
- Supports Ultra-Low Power mode (ULPM)
- Supports low-power triggers + data after trigger transmission
- Supports D-PHY initial and periodic skew calibration transactions
- Provides pre-defined error injection
- Supports driving frames from a user data file
- Provides extensive coverage, verification plan, and test suite

Simulation VIP for DSI

- Used continuously since 2008, and has verified dozens of production designs
- Fully supports both MIPI DSI℠ and DSI-2℠ protocols
- Includes VIP for MIPI D-PHY and C-PHY for physical layer verification
- Includes the DSI-2 testsuite for fast integration as part of RapidCheck IP Validator
- Includes support for Display Pixel Interface (DPI℠) and Display Bus Interface (DBI℠) protocols
- Verifies both DSI processor and peripheral
- Supports both high-speed and low-power data transmission
- Supports Ultra-Low-Power mode (ULPM)
- Provides user API to control packets with all data types
- Supports sending and receiving of DSI packets and frames in command mode and all video modes
- Supports one to four data lanes
- Provides pre-defined error injection
- Provides extensive coverage, verification plan, and test suite

Simulation VIP for I3C

- First-to-market VIP with MIPI I3C℠ support
- Complies with the latest I3C specification version
- Includes I3C testsuite for fast integration as part of RapidCheck IP Validator
- Fully supports I3C Dynamic Address Assignment procedure
- Supports In-Band Interrupts
- Supports mandatory and optional CCCs: Direct and broadcast commands
- Support for Legacy I2C Slave devices
- Supports I3C SDR mode
- Supports all I3C HDR modes: DDR, TSP, and TSL



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Cadence VIP MIPI SoundWire Frame tracker version SOUNDWIRE_1_1 for Bus 0
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  Start time     End time Opcode PREQ DevAddr RegAddr Static RegData Dynamic PAR NAK  ACK      Register Name        Errors
                                      -SBB   SlvStat        SlvStat
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        20ns      480ns  PING    0      0      0    163      0       a      0   0    0
       480ns      960ns  PING    0      0      0    163      0       5      1   0    0
       960ns     1440ns  PING    0      0      0    163      0       b      0   0    0
      1440ns     1920ns  PING    0      0      0    163      0       7      0   0    0
      1920ns     2400ns  PING    0      0      0    163      0       f      0   0    0
      2400ns     2880ns  PING    0      0      0    163      0       e      1   0    0
      2880ns     3360ns  PING    0      0      0    163      0       c      0   0    0
      3360ns     3840ns  PING    0      0      0    163      0       8      0   0    0
      3840ns     4320ns  PING    0      0      0    163      0       1      1   0    0
      4320ns     4800ns  PING    0      0      0    163      0       2      1   0    0
      4800ns     5280ns  PING    0      0      0    163      0       4      0   0    0
      5760ns     6240ns  PING    0      0      0    163      1       3      0   0    0
      6240ns     6720ns  PING    0      0      0    163      1       6      1   0    0
      6720ns     7200ns  PING    0      0      0    163      1       d      1   0    0
      7200ns     7680ns  READ    0      0     28    163      0       a      1   0    1      SCP_DevId_0
      7680ns     8160ns  READ    0      0     29    163      0       5      1   0    1      SCP_DevId_1
      8160ns     8640ns  READ    0      0     2a    163      0       b      0   0    1      SCP_DevId_2
      8640ns     9120ns  READ    0      0     2b    163      0       7      0   0    1      SCP_DevId_3
      9120ns     9600ns  READ    0      0     2c    163      4       f      0   0    1      SCP_DevId_4
      9600ns    10080ns  READ    0      0     2d    163     12       e      1   0    1      SCP_DevId_5
     10080ns    10560ns WRITE    0      0     26    163      6       c      0   0    1      SCP_DevNumber
     10560ns    11040ns  PING    0      0     10    163      1       8      0   0    0
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Figure 2: The MIPI VIP Frame Tracker enables fast protocol debugging for MIPI protocols.

Simulation VIP for M-PHY

- Complies with MIPI M-PHY® 4.1 specification
- Supports M-PHY Type 1 and Type 2
- Supports serial and signaling (RMMI) interfaces
- Supports multiple transmission speed ranges (PWM G1-G7, all Hs-GEARS) and rates per BURST mode
- Supports ACTIVATED states, SAVE states (SLEEP and STALL), and hibernate ("HIBERN8") state
- Supports distribution and merging data over one to four lanes
- Supports different number of lanes per sublink (direction)
- Generates constrained-random stimuli for data and control
- Monitors, checks, and collects coverage results
- Provides pre-defined error injection

Simulation VIP for UniPro

- Complies with MIPI UniPro℠ 1.8 specification
- Includes the MIPI M-PHY VIP for physical layer verification
- Provide comprehensive UniPro testsuite, coverage model, and verification plan as part of TripleCheck IP Validator
- Supports PHY, PA, DLL, network, and transport layers
- Supports PA link start up, (re-)initialization, configuration, and hibernate enter/exit sequences
- Supports DLL initialization, TC0 and TC1, flow control, and acknowledgement mechanisms
- Supports TL connection management and addressing, segmentation and reassembly, end-to-end flow control, and multi-CPort arbitration
- Supports up to four lanes, PWM G1-G7, HS G1-G4 on each direction, and A/B HS rate series

Simulation VIP for SoundWire

- First to market VIP with MIPI SoundWire® support
- Supports verification of SoundWire master and slave devices
- Provide comprehensive SoundWire testsuite, coverage model, and verification plan as part of TripleCheck IP Validator
- Supports emulation with up to 11 slaves, with 1 to 14 data ports per slave
- Supports initialization sequence and enumeration process
- Supports multi-lane configuration
- Supports all kinds of resets on the fly
- Supports error scenarios for Master and Slaves
- Slave VIP replies automatically when interrupt needs to be generated based on configuration
- Supports traffic flow control
- Support Block per Port and Block Per Channel packing modes

MIPI Protocols	
Protocol	**Specification**
CSI-2	v.1.3, v2.0
DSI	v1.3
DSI-2	v1.0
UniPro	v1.8
SoundWire	v1.2
SLIMbus	v2.0
I3C	v1.1
LLI	v2.0
M-PHY	v4.1
D-PHY	v2.1
C-PHY	v1.2
DBI	v2.0
DPI	v2.0
Related Protocols	
UFS (JEDEC)	v3.0
SMBus	v3.0
PMBus	v1.3.1

Table 1: MIPI protocols supported by Cadence VIP

Simulation VIP for SLIMbus

- Supports all protocol messages
- Supports MIPI SLIMbus® transport protocols (isochronous, pushed, pulled, async simplex, async half-duplex, extended asyncs)
- Supports bus reconfiguration
- Supports component boot-up sequence and recovery of sync loss
- Supports multi-channel stream
- Provides ability to change root freq and clock gear
- Supports information/value element messages
- Supports full reset flow
- Supports active framer handover flow
- Supports clock pause flows
- Supports secondary data line
- Provides comprehensive error injection

Memory Model VIP for UFS

- Boot and initialization sequence support; can be optionally skipped to save simulation time
- Supports LUNS and W-LUNS
- Supports interleaving of commands
- Supports queue depth of over 32 commands
- Supports UPIUs and SCSI commands
- Supports multiple interfaces: DpDn, RMMI, and CPort
- Backdoor loads to individual logic unit number (LUN) memories
- Backdoor access for flags, attributes, and descriptors
- Transaction and memory callbacks for all protocol and device memory events (read/write)
- Supports low-speed and high-speed transmission
- Supports nesting and Automatic Repeat request (ARQ)
- Supports NACKs and retransmissions, including dummy frames
- Enables user-controlled error injection
- Includes VIP for MIPI UniPro and M-PHY

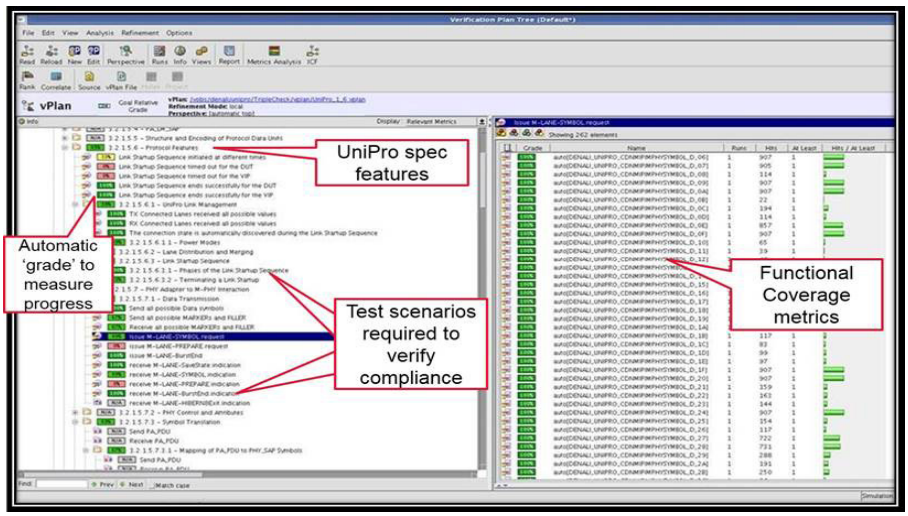

Figure 3: TripleCheck Verification Plan for MIPI UniPro

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