

VIP Catalog

Overview

Specifications for standard interface protocols are often hundreds of pages long. Deciphering these specifications and accurately modeling the protocols is a huge development effort requiring deep technical knowledge. By using production-proven Cadence® Verification IP (VIP), your system-on-chip (SoC) designs can be verified faster, more thoroughly, and with less effort.

Cadence is the industry VIP leader with products supporting more than 40 communication protocols and 60 memory interfaces. Cadence VIP fits into nearly every verification environment with support for all major simulators and verification languages. Our VIP delivers the advanced features that you need to maximize your productivity and keep projects moving forward.

A Proven Solution

There is a good chance that the devices you use every day were verified using Cadence VIP. In fact, more than 500 customers have trusted the Cadence VIP Catalog to verify thousands of designs spanning every type of electronic product.

The S.M.A.R.T. Choice

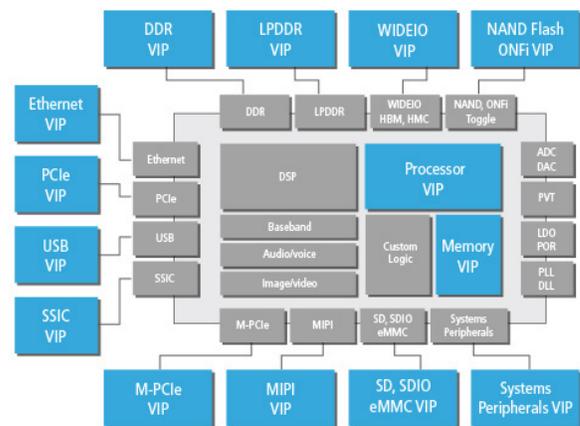
Cadence VIP is the smart choice for your next project. Customers continue to choose Cadence VIP for the unique benefits it delivers, including:

SoC-Level Verification Power

- Boost simulation performance by 100 times and more using Accelerated VIP with the Palladium XP series of hardware accelerators
- Verify conformance with SoC interconnect IP rules using Interconnect Validator
- Enable SoC latency and bandwidth analysis with Interconnect Workbench

Memory support

- Verify all your memory interfaces with Memory Models spanning: 6000 memory components, 60 types of memory interfaces, and 85 memory manufacturers



Availability of Protocols

Verify all the complex interfaces in your design with interface VIP covering more than:

- 40 communication protocols
- 60 memory interfaces

Leverage the outstanding Cadence track record of being first to market with support for new protocols

Ready-made for your environment

- Maximize the value of your simulation licenses and get consistent results whether you use the Cadence Incisive®, Synopsys VCS, or Mentor Questa simulators
- Use the verification language that you prefer. Choose from SystemVerilog, e, Verilog, VHDL, or C/C++
- Migrate to the Universal Verification Methodology (UVM) or continue using the legacy methodologies that preceded it. It's your choice!

Technically advanced features

- Perform superior protocol compliance verification with TripleCheck IP Validator
- Shorten time-to-first test with the PureView graphical configuration utility
- Use available Assertion-Based VIP for exhaustive formal verification of parallel bus protocols

"As the complexity of ARM partners' designs increases year after year, successfully verifying the performance of the SoCs has become a critical imperative. The comprehensive Cadence Verification IP solution for AMBA® protocols has enabled our mutual customers to address this challenge while incorporating the latest ARM technology. The ARM partnership with Cadence helps customers achieve continued success as they roll out next-generation designs incorporating our most advanced AMBA specifications such as AXI4 and AXI Coherency Extensions (ACE™)."

– Joe Convey, Director of Design Enablement, ARM

Simulation VIP

Cadence® Simulation VIP is the world's most widely used VIP for digital simulation. Hundreds of customers have used Cadence VIP to verify thousands of designs, from IP blocks to full systems on chip (SoCs).

The Simulation VIP is ready-made for your environment, providing consistent results whether you are using Cadence Incisive®, Synopsys VCS®, or Mentor Questa® simulators. You have the freedom to build your testbench using any of these verification languages: SystemVerilog, e, Verilog, VHDL, or C/C++. Cadence Simulation VIP supports the Universal Verification Methodology (UVM) as well as legacy methodologies.

The unique flexible architecture of Cadence VIP makes this possible. It includes a multi-language testbench interface with full access to the source code to make it easy to integrate VIP with your testbench. Optimized cores for simulation and simulation-acceleration allow you to choose the verification approach that best meets your objectives.

ARM® AMBA® 5 CHI	ARM AMBA 4 ACE	ARM AMBA AXI 3/4	ARM AMBA AHB	ARM AMBA 4 Stream	CAN	Display Port
Ethernet 10/100/1G/10G	Ethernet 40G/100G	HDMI 2.0	HDMI 1.4	I2C	JTAG incl. cJTAG	LIN
MIPI CSI-3	MIPI CSI-2	MIPI C-PHY	MIPI DigRF	MIPI D-PHY	MIPI DSI	MIPI LLI 2.0
MIPI M-PHY	MIPI SLIMbus	MIPI Sound-Wire	MIPI UniPro	NVM Express	OCP 3.0	OCP 2.2
PCI	PCIe Gen 4	PCIe Gen 3	PCIe Gen 2	PCIe SR-IOV	PCIe MR-IOV	M-PCIe
PLB 6	SAS 12G	SAS 6G	SATA 6G	SRIO	UART	USB 3.0 incl. OTG
USB 2.0 incl. OTG	USB SSIC					

Assertion-based VIP

Formal analysis is a mathematical approach to verification that has the unique ability to prove that a design is 100% correct. This method is tremendously useful, but is limited in the size and types of designs that can be verified. Still, for IP blocks with bus-style interfaces, it is an ideal verification solution.

Cadence® Assertion-Based VIP simplifies formal verification through its plug-and-play approach. Just attach the VIP to your design and run – no need for complicated tests and coverage analysis.

AMBA 4 ACE	AMBA AHB	AMBA AXI	DFI	OCP
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"AppliedMicro values working with leading IP providers, like Cadence, to help us achieve our design requirements in the most cost-effective manner. To get to market quickly with lower risk of integration errors, we chose Cadence Verification IP designed for seamless integration into our advanced SystemVerilog design and verification methodology. Cadence's performance and integration gives us confidence that our end-products will properly interoperate with these industry-standard interfaces."

– Amal Bommireddy, Vice President of Engineering, AppliedMicro

“As Cadence promised, our validation environment now runs hundreds of times faster than with simulation. Accelerated VIP running on the Palladium® XP (platform) increased my team’s productivity by 100%. It also enabled us to find bugs we were unable to reach using simulation.”

– Tony Gladwin George, Verification Engineer, Samsung

Memory Models

Memory is a major part of every electronic product. Every system on chip (SoC) contains embedded memories and must also interface with external memory components. The operation of these interfaces impacts both SoC functionality and performance, making memory interface verification a crucial step in the SoC development process.

Cadence® Memory Models are the gold standard for memory interface verification. Used by more than 500 customers, Cadence Memory Models provide support for 6,000 memories spanning 60 memory interface types and 85 memory manufacturers.

DDR3	DDR4	eMMC 4.5	eMMC 5.0	Flash ONFi 3.0	Flash Toggle NAND 2
LPDDR3	LPDDR4	LRDIMM	DDR4 LRDIMM	Flash PPN DDR	SD Card 4.0
UFS 2.0	Wide I/O	Wide I/O 2			

Accelerated VIP

Sometimes chips are just too big to verify with logic simulation software. SoCs comprised of tens of millions of logic gates will bog down software simulators, even when running on the fastest servers.

Simulating big designs requires hardware-assisted verification, an approach that uses special-purpose hardware, like Cadence® Palladium® XP systems, to dramatically boost simulation performance.

Just as simulation VIP simplifies traditional logic simulation, accelerated VIP makes hardware-assisted verification easier and more productive.

AMBA 4 ACE	AMBA AXI	AMBA AHB	AMBA APB	Ethernet 10/100/1G/10G	HDMI 1.4
12C	12S	Keypad	MIPI CSI-2	MIPI DBI	MIPI DSI
PCI Express Gen 2/ Gen 3	SATA 3G/6G	SIMCARD			

“The HDMI 2.0 Verification IP provided by Cadence enabled a small verification team to deliver reliable results within very tight schedule constraints. By reducing the effort required to develop a verification solution, our engineers were able to focus on other tasks crucial to project completion. As a result, we were able to create the type of high-quality and reliable design expected by our customers.”

– Larry Porter, Verification Manager, Display Products Division, STMicroelectronics

Productivity Tools

System-on-chip (SoC) verification is a big job. That's why high-level verification languages like e and SystemVerilog were developed along with companion methodologies like the Universal Verification Methodology (UVM). But language and methodology only take you so far.

Cadence provides additional productivity-boosting tools to help you configure, run, and analyze your design. With these products, you get up and running quickly and shorten your overall verification project.

PureView

PureView is a graphical cockpit used to configure all our VIP products. Many interface protocols have dozens of configuration options. To match a VIP component to your design, each option needs to be set correctly. It would be time-consuming and error-prone to set every parameter with a text command, but PureView makes it easy. The tool walks you through a hierarchy of menus to configure a VIP component. It only shows you relevant options based on previous choices and prevents illegal settings. PureSuite is also used to configure memory model options and TripleCheck tests.

TripleCheck for PCI Express and Ethernet 40G/100G

TripleCheck for PCI Express helps you verify that your design complies with the interface specification. This is different than a post-silicon compliance test that measures electrical parameters. TripleCheck works during pre-silicon logic simulation to stress-test functional behavior. TripleCheck is the third-generation compliance product to be offered by Cadence, delivering an enhanced test suite, coverage model, and verification plan.

Interconnect Solution

Many SoCs now employ sophisticated interconnect fabric IP to link multiple processor cores, caches, memories, and dozens of other IP blocks. These interconnect fabrics are enabling new generations of low-power servers and high-performance mobile devices. However, sophisticated interconnects are highly configurable, and that creates design challenges.

It can be difficult to verify that master and slave components are adhering to cache coherency rules. Also, seemingly minor variations in interconnect configuration can introduce unintended bottlenecks that choke SoC performance.

The Cadence® Interconnect Solution is designed to meet the needs of verification engineers and system architects by simplifying the verification of interconnect data integrity and identifying performance bottlenecks before they are locked in silicon. The solution includes the Cadence Interconnect Validator and Cadence Interconnect Workbench.

Interconnect Validator

Cadence Interconnect Validator verifies the correctness and completeness of data as it passes through the SoC interconnect fabric. Because it automates a critical, yet difficult and time-consuming task, Interconnect Validator greatly increases your productivity. Interconnect Validator reduces verification effort by automatically creating a coverage model of all transactions exchanged between masters and slaves within an SoC. It includes a passive agent to monitor the SoC interconnect as well as an active agent to model interconnect behavior and enable SoC verification in cases where the interconnect design is not yet complete.

Because interconnect behavior is always design-specific, Interconnect Validator can be extended and customized to enable design-specific checking. User-created rules can be added and standard protocol rules can be bypassed.

Interconnect Workbench

Your interconnect sub-system might be functionally correct, but are you starving your IP blocks of the bandwidth they need? Is the data from latency-critical blocks getting through on time? With the Cadence Interconnect Workbench, answering these questions becomes much easier. The solution collects cycle-accurate traffic from multiple simulation runs and displays latency and bandwidth measurements in an easy-to-use performance cockpit.



Cadence Design Systems enables global electronic design innovation and plays an essential role in the creation of today's electronics. Customers use Cadence software, hardware, IP, and expertise to design and verify today's mobile, cloud, and connectivity applications. www.cadence.com

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