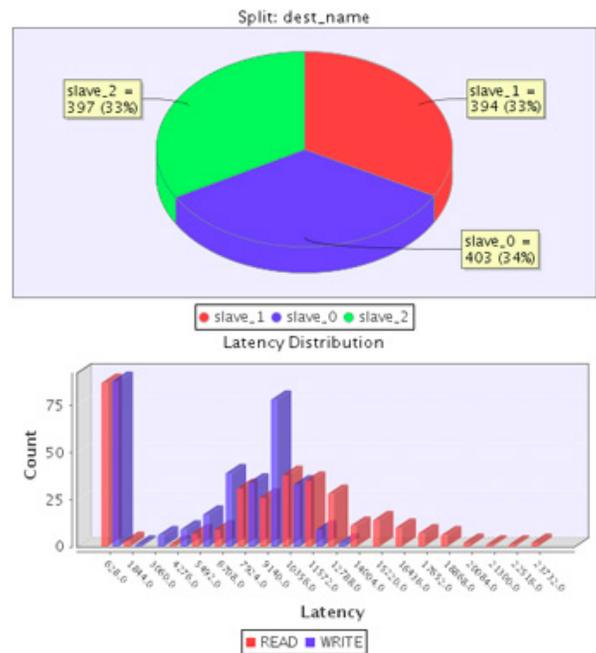# Interconnect Solution

Overview

Many SoCs now employ sophisticated interconnect fabric IP to link multiple processor cores, caches, memories, and dozens of other IP blocks. These interconnect fabrics are enabling new generations of low-power servers and high-performance mobile devices. However, sophisticated interconnects are highly configurable, and that creates design challenges.

It can be difficult to verify that master and slave components are adhering to cache coherency rules. Also, seemingly minor variations in interconnect configuration can introduce unintended bottlenecks that choke SoC performance.

The Cadence® Interconnect Solution is designed to meet the needs of verification engineers and system architects by simplifying the verification of interconnect data integrity and identifying performance bottlenecks before they are locked in silicon. The solution includes the Cadence Interconnect Validator and Cadence Interconnect Workbench.

Interconnect Validator

Cadence Interconnect Validator verifies the correctness and completeness of data as it passes through the SoC interconnect fabric. Because it automates a critical, yet difficult and time-consuming task, Interconnect Validator greatly increases your productivity. Interconnect Validator reduces verification effort by automatically creating a coverage model of all transactions exchanged between masters and slaves within an SoC. It includes a passive agent to monitor the SoC interconnect as well as an active agent to model interconnect behavior and enable SoC verification in cases where the interconnect design is not yet complete.

Because interconnect behavior is always design-specific, Interconnect Validator can be extended and customized to enable design-specific checking. User-created rules can be added and standard protocol rules can be bypassed.

Interconnect Validator (Basic)

The Interconnect Validator (Basic) product is used to verify non-coherent interconnect fabrics like ARM's NIC-400 System IP.

The solution:

- Supports any number of masters and slaves
- Accommodates independent address forwarding for each master
- Handles data splitting, upsizing, and downsizing
- Supports INCR, WRAP, and FIXED addressing modes
- Supports internal address ranges and unmapped access
- Supports transaction ordering
- Handles slave power-down, interconnect reset, and dynamic address forwarding

Interconnect Validator (Coherent)

The Interconnect Validator (Coherent) product is used to verify coherent interconnect fabrics like the ARM® CCI-400 System IP.

The solution:

- Supports any number of outer and inner domains
- Verifies snoop conversions, snoop propagation, and snoop filter operation
- Checks cross-cache line operations
- Supports DVM transactions
- Verifies barrier transactions
- Supports interconnect-initiated operations
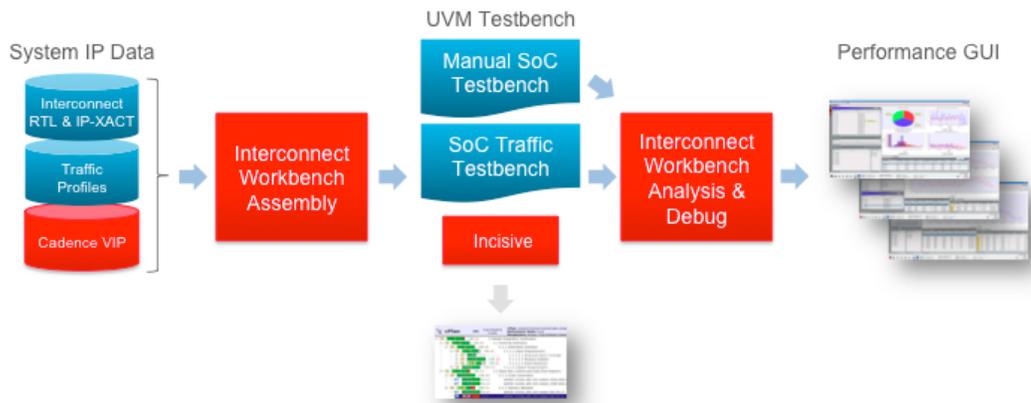
Interconnect Workbench

Your interconnect sub-system might be functionally correct, but are you starving your IP blocks of the bandwidth they need? Is the data from latency-critical blocks getting through on time? With the Cadence Interconnect Workbench, answering these questions becomes much easier. The solution collects cycle-accurate traffic from multiple simulation runs and displays latency and bandwidth measurements in an easy-to-use performance cockpit.

Performance Analysis Cockpit

The performance analysis cockpit makes it easy to visualize, discover, and debug system performance behaviors. Features include:

- Shaping of interface traffic with sequences to assess system performance under various traffic loads
- Click-through aggregated traffic results to pinpoint outlier transactions and debug in the waveform viewer
- Performance-sensitivity analysis to compare various implementation options and quality-of-service configurations

Automatic Test Bench Creation

Your interconnect fabric may have dozens of masters and hundreds of slaves. Or, you might have an environment where you're undergoing a tight iteration of running, analyzing, and tweaking the configuration of a much smaller interconnect. Building and re-building the testbench to analyze each configuration is a tedious and error-prone process.

Interconnect Workbench saves time and frustration by automatically generating testbenches. It imports interconnect fabric RTL and IP-XACT metadata from the ARM CoreLink™ AMBA® Designer product, builds either a performance-oriented testbench or a verification-oriented testbench, and builds a basic test suite.