

Wide I/O Memory Model

Overview

Memory is a major part of every electronic product. Every system on chip (SoC) contains embedded memories and must also interface with external memory components. The operation of these interfaces impacts both SoC functionality and performance, making memory interface verification a crucial step in the SoC development process.

Cadence® Memory Models are the gold standard for memory interface verification. Used by more than 500 customers, Cadence Memory Models provide support for 6,500 memories spanning 60 memory interface types and 85 memory manufacturers.



Vendor Certification

Memory models for commercial memory components are based on the manufacturer's datasheets and are then provided to the manufacturer for certification. This closed-loop quality control process means that you can trust your simulation results. Models for new external memory standards that do not yet have commercial component providers and models for internal memory standards are based upon the specifications provided by the controlling standards body, such as JEDEC, ONFI, and SD Association. Cadence works closely with our early-adopter customers to ensure the quality of these models.

Accurate Timing Analysis

When memory models represent actual memory chips and modules, the memory models include full timing parameters that support accurate gate-level simulations. Timing specs are conveniently displayed in the PureView tool and can be overridden for what-if analysis.

Second Source Evaluation

Memory models are inserted into a testbench as generic models that are then associated with a personality file to represent a specific component. This makes it easy to do second-source evaluation of memory components.

Specification Support

Our Wide I/O SDRAM Memory Model VIP supports single-channel implementation of the officially released JESD229 version of the Wide I/O SDR specification, and can be used four times to model the 4-channel device.

Key Features

- Implements internal Wide I/O state machine and performs specified timing checks.
- 128-bit wide data bus. Single data rate.
- The model supports a wide range of device densities.
- Differential CK/DQS allowed for future DDR extension.
- Refresh allows portions of the array to be powered down when not required, permitting applications to determine device memory requirements on a real-time usage basis.



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