LRDIMM Memory Model

Overview

Memory is a major part of every electronic product. Every system on chip (SoC) contains embedded memories and must also interface with external memory components. The operation of these interfaces impacts both SoC functionality and performance, making memory interface verification a crucial step in the SoC development process.

Cadence® Memory Models are the gold standard for memory interface verification. Used by more than 500 customers, Cadence Memory Models provide support for 6,500 memories spanning 60 memory interface types and 85 memory manufacturers.

Vendor Certification

 Memory models for commercial memory components are based on the manufacturer's datasheets and are then provided to the manufacturer for certification. This closed-loop quality control process means that you can trust your simulation results. Models for new external memory standards that do not yet have commercial component providers and models for internal memory standards are based upon the specifications provided by the controlling standards body, such as JEDEC, ONFi, and SD Association. Cadence works closely with our early-adopter customers to ensure the quality of these models.

Accurate Timing Analysis

When memory models represent actual memory chips and modules, the memory models include full timing parameters that support accurate gate-level simulations. Timing specs are conveniently displayed in the PureView tool and can be overridden for what-if analysis.

Second Source Evaluation

Memory models are inserted into a testbench as generic models that are then associated with a personality file to represent a specific component. This makes it easy to do second-source evaluation of memory components.

Specification Support

Our DDR RDIMM Memory Model VIP supports JEDEC DDR3 SDRAM Registered DIMM Design Specification Revision 0.84, as well as LRDIMM Specification Memory Buffer (Rev 0.95a) and JEDEC DDR3 Register - JESD82-29A for SSTE32882 (the RCD) specification.

Key Features

- Number of ranks and components constituting the DIMM are configurable using SOMA files.

- A DRAM instantiation for checks bits is optionally available.

- Models both the Power Up Reset and Reset with Stable Power with all timing and pin validity checks.

- Controller can do CWW and set bits to change most of the control word settings.

- Supports of fly by delays DIMM to DRAM (for UDIMM) and RCD to DRAM (for RDIMM/LRDIMM).

- RDIMM will optionally mirror address bits (as mentioned in the specification).

- DRAM MRS command handling, Inversion, Mirroring, Command Latency, propagation delay, gating with parity checks, different CS modes, etc.

- Supports optional checking for even parity in case of errors gating CWW and DRAM commands defined in the spec.

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