VIP Datasheet

LPDDR4 Memory Model

Overview

Memory is a major part of every electronic product. Every system on chip (SoC) contains embedded memories and must also interface with external memory components. The operation of these interfaces impacts both SoC functionality and performance, making memory interface verification a crucial step in the SoC development process.

Cadence® Memory Models are the gold standard for memory interface verification. Used by more than 500 customers, Cadence Memory Models provide support for 6,500 memories spanning 60 memory interface types and 85 memory manufacturers.

Vendor Certification

Memory models for commercial memory components are based on the manufacturer's datasheets and are then provided to the manufacturer for certification. This closed-loop quality control process means that you can trust your simulation results. Models for new external memory standards that do not yet have commercial component providers and models for internal memory standards are based upon the specifications provided by the controlling standards body, such as JEDEC, ONFi, and SD Association. Cadence works closely with our early-adopter customers to ensure the quality of these models.

Accurate Timing Analysis

When memory models represent actual memory chips and modules, the memory models include full timing parameters that support accurate gate-level simulations. Timing specs are conveniently displayed in the PureView tool and can be overridden for what-if analysis.

Second Source Evaluation

Memory models are inserted into a testbench as generic models that are then associated with a personality file to represent a specific component. This makes it easy to do second-source evaluation of memory components.

Specification Support

The LPDDR4 Memory Model VIP is evolving and supports the most of the proposals that are balloted at JEDEC.

Key Features

- Support 2 channels which can function independently
- Precharge, Activate, Read, Write, Mask Write, Mode Register Read, Mode Register Write, Power Down,Refresh, Self Refresh and related timing checks
- Supports a wide range of device densities from 4Gb to 32 Gb
- Speed (Mt/s): 2133 MHz (4266 MT/s)
- Data on the bus can be inverted during both read and write to save power. Both Data Mask and Data Bus inversion features can be set through mode registers
- Bust length during Read, Write and Mask Write can be set on the fly through command data and mode registers
- Allows preamble and postamble to be configured for Read, Write and Mask Write
- Allows LPDDR4 to be switched between two differing operating frequencies by duplicating mode register parameters commonly changed with operating frequency
- Supports Read FIFO and Write FIFO commands used during Write training
- Supports all 7 MPC commands
- The training centers the internal VREF(ca) in the CA data eye and, at the same time, allows for timing adjustments of the CS and CA signals to meet setup/hold requirements.
- Supports and checks all read and write latencies requirements for a given frequency
- Support CA and DQ voltage reference settings
- Supports all combinations of Reads merging and Writes merging placed Tccd+n apart

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