VIP Datasheet

eMMC 5.0 Memory Model

Overview

Memory is a major part of every electronic product. Every system on chip (SoC) contains embedded memories and must also interface with external memory components. The operation of these interfaces impacts both SoC functionality and performance, making memory interface verification a crucial step in the SoC development process.

Cadence® Memory Models are the gold standard for memory interface verification. Used by more than 500 customers, Cadence Memory Models provide support for 6,500 memories spanning 60 memory interface types and 85 memory manufacturers.

Vendor Certification

Memory models for commercial memory components are based on the manufacturer's datasheets and are then provided to the manufacturer for certification. This closed-loop quality control process means that you can trust your simulation results. Models for new external memory standards that do not yet have commercial component providers and models for internal memory standards are based upon the specifications provided by the controlling standards body, such as JEDEC, ONFi, and SD Association. Cadence works closely with our early-adopter customers to ensure the quality of these models.

Accurate Timing Analysis

When memory models represent actual memory chips and modules, the memory models include full timing parameters that support accurate gate-level simulations. Timing specs are conveniently displayed in the PureView tool and can be overridden for what-if analysis.

Second Source Evaluation

Memory models are inserted into a testbench as generic models that are then associated with a personality file to represent a specific component. This makes it easy to do second-source evaluation of memory components.

Specification Support

Supports the eMMC 5.0 and 5.1 specification

Key Features

- Implements register bit definitions for a subset of eMMC standard bit definitions.
- Checks for proper initialization sequence. This check can be skipped.
- Implements internal eMMC state machine and performs specified timing checks.
- Implements Cache Read/Write operations per the eMMC JEDEC specification
- Implements Data tag mechanism per eMMC JEDEC spec.
- Implements Discard operation per eMMC JEDEC spec
- Implements 200 MB/s Read/Write operation
- Implements Read/Write operations for large 4Kb sector sizes
- Supports notification mechanism when the host intends to power off the device
- Implements Replay Protected Memory Block functionality per the eMMC JEDEC spec
- Implements HS400 Dual Data Rate Read and Write interface per eMMC 5.0 JEDEC spec.
- For devices larger than 2GB, the addressing mechanism is switched from byte addressing to sector addressing.
- Implements 48 bit input command format and R1, R1b, R2, etc. response formats.
- As part of the CMD1 operation, the model will implement voltage range negotiation.
- Implements the Context Management functionality per the eMMC JEDEC spec
- Supports Dual Data Rate timing mode for Read/Write operations, reading CID and CSD registers, sending CRC status and Boot acknowledge
- Implements Extended Partition Types operation per eMMC JEDEC spec.
- Supports High Priority Interrupt mechanism
- Implements Packed Read/Write operation per eMMC JEDEC spec.
- Supports accepting Real Time Clock Information the host sends to the card
- Implements Sanitize operation per eMMC JEDEC spec.
- Added a new signal “Data Strobe” which directs bit transfer on data lines in HS400 mode.

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