

DDR4 LRDIMM Memory Model

Overview

Memory is a major part of every electronic product. Every system on chip (SoC) contains embedded memories and must also interface with external memory components. The operation of these interfaces impacts both SoC functionality and performance, making memory interface verification a crucial step in the SoC development process.

Cadence® Memory Models are the gold standard for memory interface verification. Used by more than 500 customers, Cadence Memory Models provide support for 6,500 memories spanning 60 memory interface types and 85 memory manufacturers.



Vendor Certification

Memory models for commercial memory components are based on the manufacturer's datasheets and are then provided to the manufacturer for certification. This closed-loop quality control process means that you can trust your simulation results. Models for new external memory standards that do not yet have commercial component providers and models for internal memory standards are based upon the specifications provided by the controlling standards body, such as JEDEC, ONFI, and SD Association. Cadence works closely with our early-adopter customers to ensure the quality of these models.

Accurate Timing Analysis

When memory models represent actual memory chips and modules, the memory models include full timing parameters that support accurate gate-level simulations. Timing specs are conveniently displayed in the PureView tool and can be overridden for what-if analysis.

Second Source Evaluation

Memory models are inserted into a testbench as generic models that are then associated with a personality file to represent a specific component. This makes it easy to do second-source evaluation of memory components.

Specification Support

DDR4 LRDIMM Memory Model VIP supports JEDEC DDR4 SDRAM Registered DIMM Design Specification(Rev 0.8) for RDIMM specification and follows JEDEC DDR4 Register - DDR4RCD01 - Rev 0.92 for the RCD specification.

Key Features

- Support for signal strength modeling. Users can use pull up or pull down on the inout pins and the model will be able to detect the signal strength and function like a real device.
- Supports DDR4 UDIMM, RDIMM, LRDIMM, DDR4 3DS, 3DS UDIMM, 3DS RDIMM and 3DS LRDIMM types.
- Raw Cards with CB bits mapped to middle of DQ/DQS buses
- Number of ranks and components with and the overall interconnect between DIMM, RCD and DRAM are configurable using SOMAs.
- Can optionally have a DRAM instantiation for checks bits.
- RDIMM will optionally mirror the address bits as mentioned in specification.
- Configurable DQ Maps to match one of the options mentioned in the specification.
- Models both with the Power Up Reset and Reset with Stable Power with all timing and pin validity checks.
- DRAM MRS command handling, inversion, mirroring, command latency, propagation delay, gating with parity checks, and different cs modes.
- MRS7 interface for CWW and most of the control word settings.
- Supports optionally checking for even parity
- In case of errors gating supports CWW and DRAM commands.
- Implements different recovery mechanisms defined in the specification.
- Support Clk to CA and ODT, CKE, CSBAR loop-back modes.



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